THALES

# Cinterion® ELS61-E R2

Hardware Interface Description

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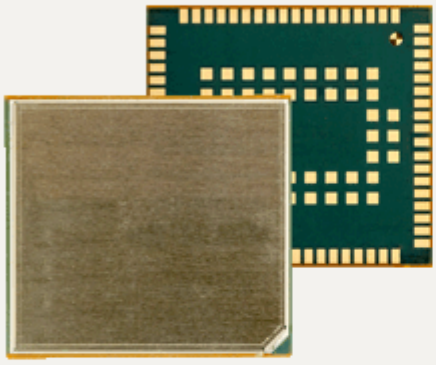

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# 1 Introduction

This document[1] describes the hardware of the Cinterion® ELS61-E R2 module. It helps you quickly retrieve interface specifications, electrical and mechanical details and information on the requirements to be considered for integrating further components.

## 1.1 Key Features at a Glance

| Feature | Implementation |
|---|---|
| *General* | |
| Frequency bands | GSM/GPRS/EDGE: Dual band 900/1800MHz<br>UMTS/HSPA+: Dual band 900 (BdVIII) / 2100MHz (BdI)<br>LTE: Penta band 700 (Bd28) / 800 (Bd20) / 900 (Bd8) / 1800 (Bd3) / 2100 MHz (Bd1) |
| GSM class | Small MS |
| Output power (according to Release 99) | Class 4 (+33dBm ±2dB) for EGSM900<br>Class 1 (+30dBm ±2dB) for GSM1800<br>Class E2 (+27dBm ± 3dB) for GSM 900 8-PSK<br>Class E2 (+26dBm +3 /-4dB) for GSM 1800 8-PSK |
| Output power (according to Release 99) | Class 3 (+23.5dBm +1.5/-2.5dB) for UMTS 2100,WCDMA FDD BdI<br>Class 3 (+23.5dBm +1.5/-2.5dB) for UMTS 900, WCDMA FDD BdVIII |
| Output power (according to Release 8) | Class 3 (+23dBm +1dB/-2dB) for LTE 700, LTE FDD Bd28<br>Class 3 (+23dBm +1dB/-2dB) for LTE 800, LTE FDD Bd20<br>Class 3 (+23dBm +1dB/-2dB) for LTE 900, LTE FDD Bd8<br>Class 3 (+23dBm +1dB/-2dB) for LTE 1800, LTE FDD Bd3<br>Class 3 (+23dBm +1dB/-2dB) for LTE 2100, LTE FDD Bd1 |
| Power supply | 3.0V to 4.5V |
| Operating temperature (board temperature) | Normal operation: -30°C to +85°C<br>Extended operation: -40°C to +90°C |
| Physical | Dimensions: 27.6mm x 25.4mm x 2.2mm<br>Weight: approx. 3.5g |
| RoHS | All hardware components fully compliant with EU RoHS Directive |
| *LTE features* | |
| 3GPP Release 9 | UE CAT 1 supported<br>DL 10.2Mbps, UL 5.2Mbps |
| *HSPA features* | |
| 3GPP Release 8 | DL 7.2Mbps, UL 5.7Mbps<br>HSDPA Cat.8 / HSUPA Cat.6 data rates<br>Compressed mode (CM) supported according to 3GPP TS25.212 |

1. The document is effective only if listed in the appropriate Release Notes as part of the technical documentation delivered with your Thales product.

| Feature | Implementation |
|---|---|
| *UMTS features* | |
| 3GPP Release 4 | PS data rate – 384 kbps DL / 384 kbps UL<br>CS data rate – 64 kbps DL / 64 kbps UL |
| *GSM/GPRS/EGPRS features* | |
| Data transfer | GPRS:<br>• Multislot Class 12<br>• Full PBCCH support<br>• Mobile Station Class B<br>• Coding Scheme 1 – 4<br>EGPRS:<br>• Multislot Class 12<br>• EDGE E2 power class for 8 PSK<br>• Downlink coding schemes – CS 1-4, MCS 1-9<br>• Uplink coding schemes – CS 1-4, MCS 1-9<br>• SRB loopback and test mode B<br>• 8-bit, 11-bit RACH<br>• PBCCH support<br>• 1 phase/2 phase access procedures<br>• Link adaptation and IR<br>• NACC, extended UL TBF<br>• Mobile Station Class B |
| SMS | Point-to-point MT and MO<br>Cell broadcast<br>Text and PDU mode<br>Storage: SIM card plus SMS locations in mobile equipment |
| *Software* | |
| AT commands | Hayes 3GPP TS 27.007, TS 27.005, Thales<br>AT commands for RIL compatibility |
| Java™ Open Platform | Java™ Open Platform with<br>• Java™ profile IMP-NG & CLDC 1.1 HI<br>• Secure data transmission via HTTPS/SSL[1]<br>• Multi-threading programming and multi-application execution<br><br>Major benefits: seamless integration into Java applications, ease of programming, no need for application microcontroller, extremely cost-efficient hardware and software design – ideal platform for industrial applications.<br><br>The memory space available for Java programs is 30MB in the flash file system and 18MB RAM. Application code and data share the space in the flash file system and in RAM. |
| Microsoft™ compatibility | RIL for Pocket PC and Smartphone |
| SIM Application Toolkit | SAT letter classes b, c, e; with BIP |
| Firmware update | Generic update from host application over ASC0 or USB modem. |

| Feature | Implementation |
|---|---|
| *Interfaces* | |
| Module interface | Surface mount device with solderable connection pads (SMT application interface). Land grid array (LGA) technology ensures high solder joint reliability and allows the use of an optional module mounting socket.<br><br>For more information on how to integrate SMT modules see also [4]. This application note comprises chapters on module mounting and application layout issues as well as on additional SMT application development equipment. |
| USB | USB 2.0 High Speed (480Mbit/s) device interface, Full Speed (12Mbit/s) compliant |
| 2 serial interfaces | ASC0 (shared with GPIO lines):<br>• 8-wire modem interface with status and control lines, unbalanced, asynchronous<br>• Adjustable baud rates: 1,200bps to 3Mbps<br>• Autobauding: 1,200bps to 230,400bps<br>• Supports RTS0/CTS0 hardware flow control.<br>ASC1 (shared with GPIO lines):<br>• 4-wire, unbalanced asynchronous interface<br>• Adjustable baud rates: 1,200bps to 921,60bps<br>• Autobauding: 1,200bps to 230,400bps<br>• Supports RTS1/CTS1 hardware flow control |
| Audio | 1 digital audio interface (DAI), shared with GPIO lines |
| UICC interface | Supported SIM/USIM cards: 3V, 1.8V |
| GPIO interface | 22 GPIO lines comprising:<br>13 lines shared with ASC0, ASC1 and SPI lines, with network status indication, PWM functionality, fast shutdown and pulse counter<br>5 GPIO lines shared with DAI interface<br>4 GPIO lines not shared |
| $I^2C$ interface | Supports $I^2C$ serial interface |
| SPI interface | Serial peripheral interface, shared with GPIO lines |
| Antenna interface pads | 50Ω. GSM/LTE main antenna, LTE Rx Diversity antenna |
| *Power on/off, Reset* | |
| Power on/off | Switch-on by hardware signal ON<br>Switch-off by AT command<br>Switch off by hardware signal FST_SHDN instead of AT command<br>Automatic switch-off in case of critical temperature or voltage conditions |
| Reset | Orderly shutdown and reset by AT command<br>Emergency reset by hardware signal EMERG_RST |
| *Special features* | |
| Real time clock | Timer functions via AT commands |
| TTY/CTM support | Integrated CTM modem |
| *Evaluation kit* | |
| Evaluation module | ELS61-E R2 module soldered onto a dedicated PCB that can be connected to an adapter in order to be mounted onto the DSB75. |

| Feature | Implementation |
|---|---|
| DSB75 | DSB75 Development Support Board designed to test and type approve Thales modules and provide a sample configuration for application engineering. A special adapter is required to connect the ELS61-E R2 evaluation module to the DSB75. |

1. HTTP/SecureConnection over SSL version 3.0 and TLS versions 1.0, 1.1, and 1.2 are supported. For details please refer to Java User's Guide for Cinterion® ELS61-E.

## 1.2 ELS61-E R2 System Overview

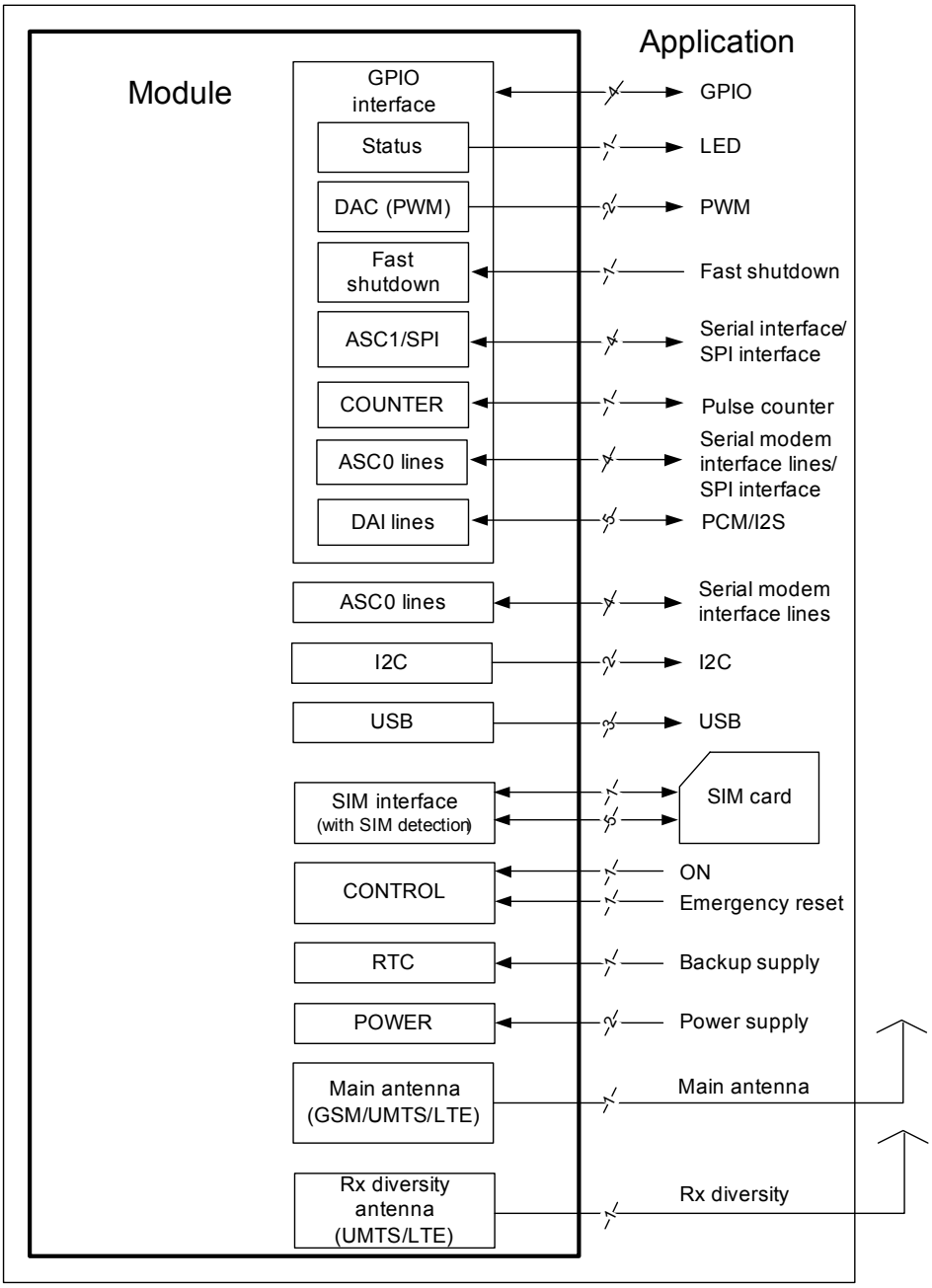



**Figure 1:** ELS61-E R2 system overview

# 1.3 Circuit Concept

Figure 2 and Figure 3 show block diagrams of the ELS61-E R2 module and illustrate the major functional components:

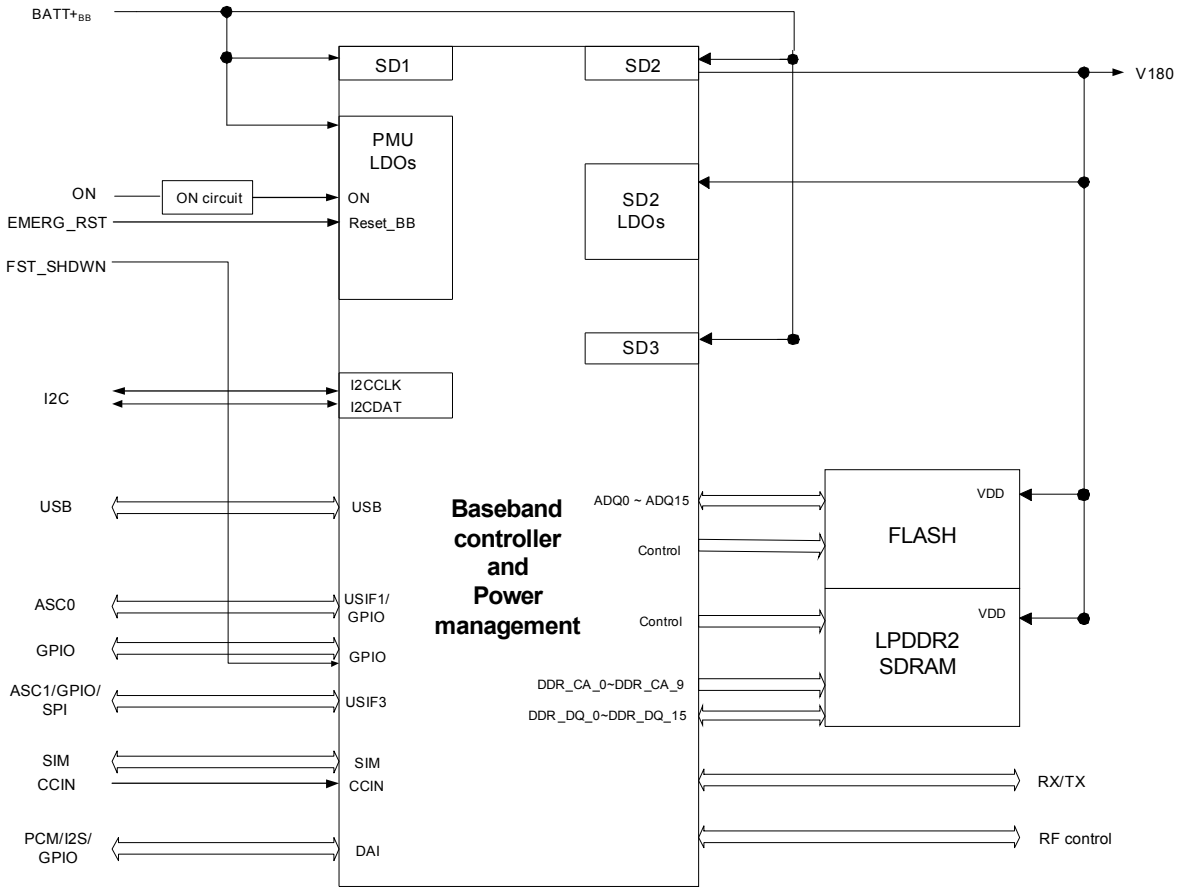



**Figure 2:** ELS61-E R2 block diagram

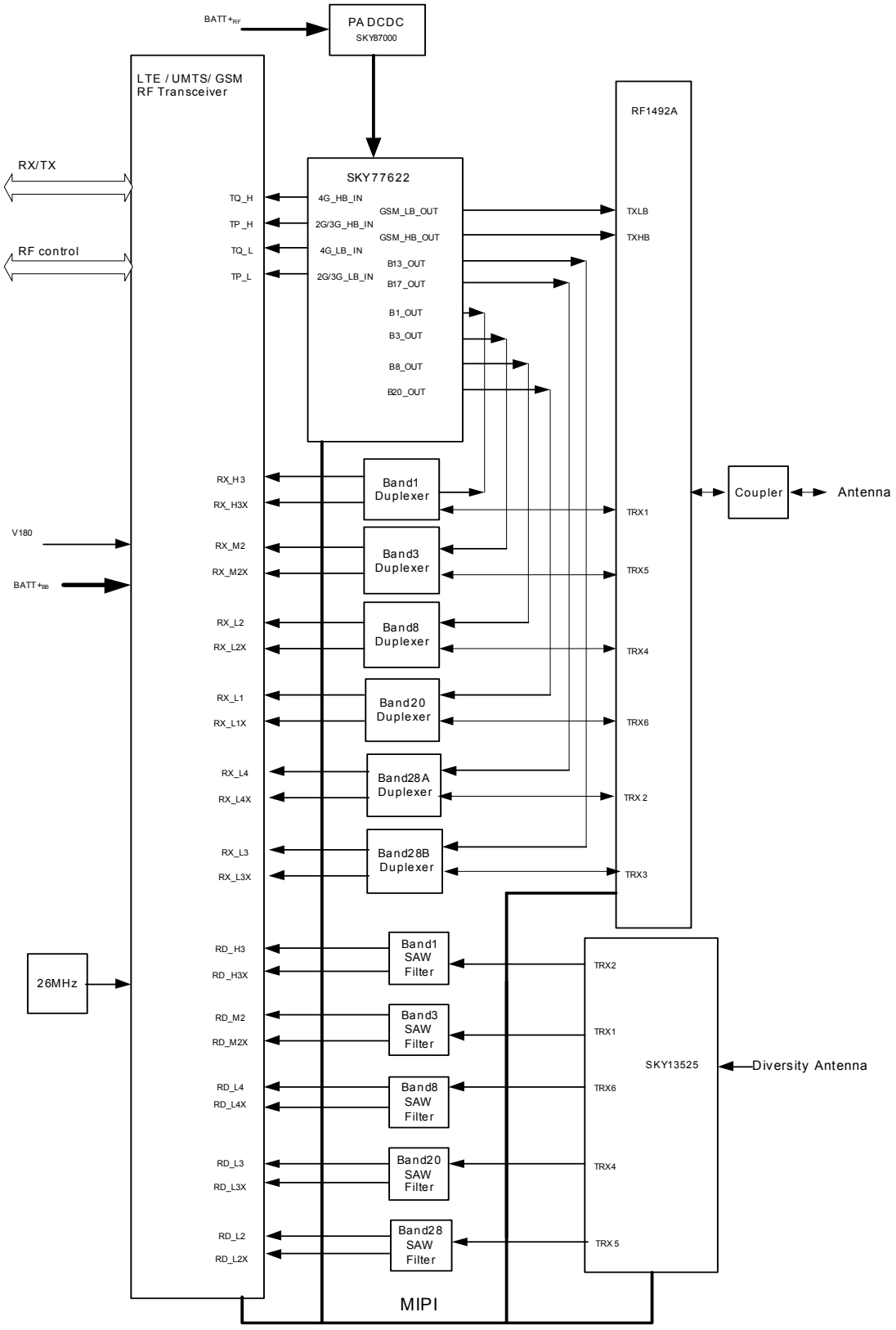



**Figure 3:** ELS61-E R2 RF section block diagram

# 2 Interface Characteristics

ELS61-E R2 is equipped with an SMT application interface that connects to the external application. The SMT application interface incorporates the various application interfaces as well as the RF antenna interface.

## 2.1 Application Interface

### 2.1.1 Pad Assignment

The SMT application interface on the ELS61-E R2 provides connecting pads to integrate the module into external applications. Figure 4 shows the connecting pads' numbering plan, the following Table 1 lists the pads' assignments.

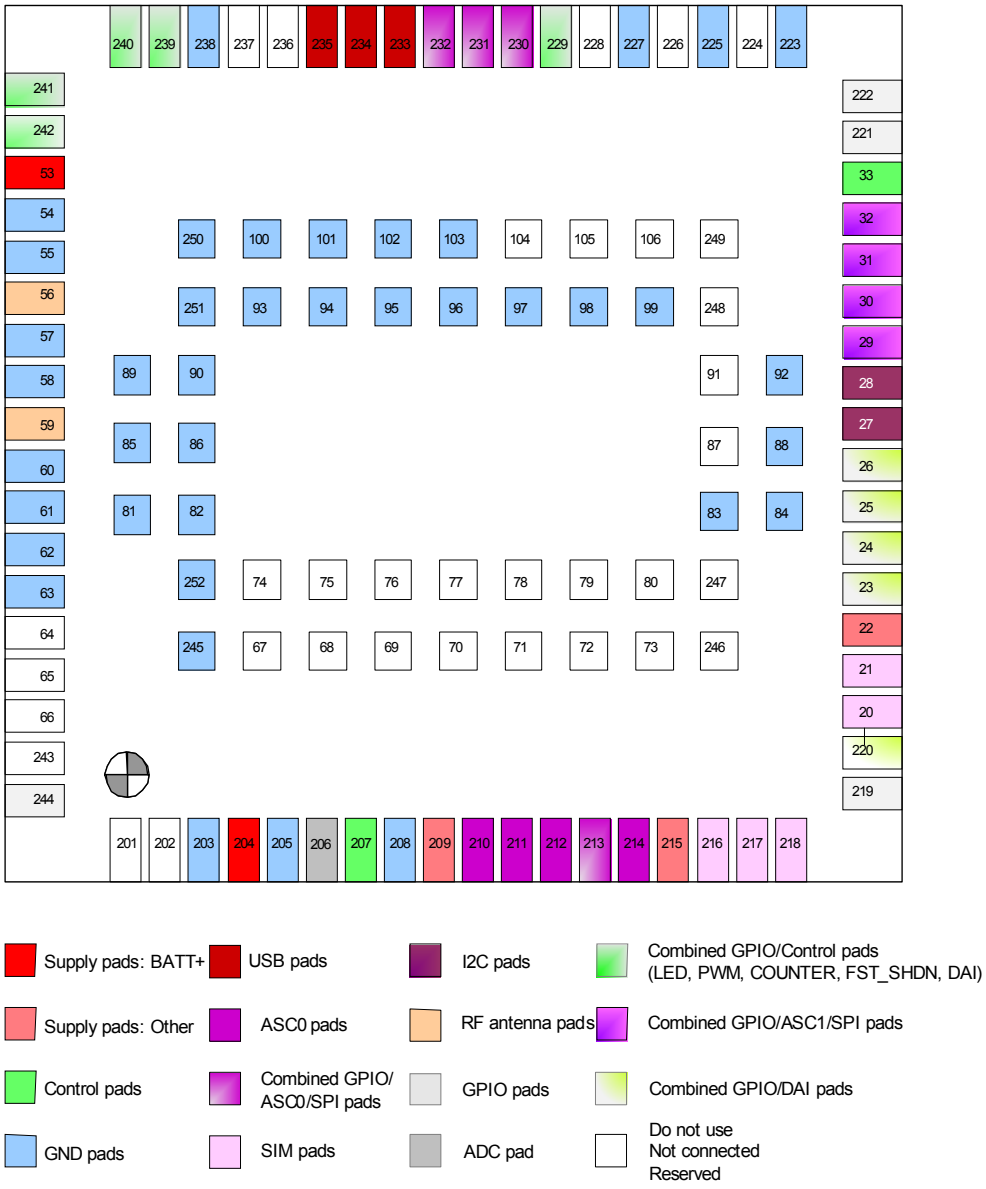



**Figure 4:** Numbering plan for connecting pads (bottom view)

**Table 1:** Pad assignments

| Pad no. | Signal name | Pad no. | Signal name | Pad no. | Signal name |
|---|---|---|---|---|---|
| 201 | Not connected | 24 | GPIO22/FSC | 235 | USB_DN |
| 202 | Not connected | 25 | GPIO21/DIN | 236 | Not connected |
| 203 | GND | 26 | GPIO23/BCLK | 237 | Not connected |
| 204 | $BATT+_{BB}$ | 27 | I2CDAT | 238 | GND |
| 205 | GND | 28 | I2CCLK | 239 | GPIO5/LED |
| 206 | ADC1 | 29 | GPIO17/TXD1/MISO | 240 | GPIO6/PWM2 |
| 207 | ON | 30 | GPIO16/RXD1/MOSI | 241 | GPIO7/PWM1 |
| 208 | GND | 31 | GPIO18/RTS1 | 242 | GPIO8/COUNTER |
| 209 | V180 | 32 | GPIO19/CTS1/SPI_CS | 53 | $BATT+_{RF}$ |
| 210 | RXD0 | 33 | EMERG_RST | 54 | GND |
| 211 | CTS0 | 221 | GPIO12 | 55 | GND |
| 212 | TXD0 | 222 | GPIO11 | 56 | ANT_DRX |
| 213 | GPIO24/RING0 | 223 | GND | 57 | GND |
| 214 | RTS0 | 224 | Not connected | 58 | GND |
| 215 | VDDLP | 225 | GND | 59 | ANT_MAIN |
| 216 | CCRST | 226 | Not connected | 60 | GND |
| 217 | CCIN | 227 | GND | 61 | GND |
| 218 | CCIO | 228 | Not connected | 62 | GND |
| 219 | GPIO14 | 229 | GPIO4/FST_SHDN/MCLK[1] | 63 | GND |
| 220 | GPIO13/MCLK[1] | 230 | GPIO3/DSR0/SPI_CLK | 64 | Not connected |
| 20 | CCVCC | 231 | GPIO2/DCD0 | 65 | Not connected |
| 21 | CCCLK | 232 | GPIO1/DTR0 | 66 | Not connected |
| 22 | VCORE | 233 | VUSB | 243 | Not connected |
| 23 | GPIO20/DOUT | 234 | USB_DP | 244 | GPIO15 |
| Centrally located pads | | | | | |
| 67 | Not connected | 83 | GND | 99 | GND |
| 68 | Not connected | 84 | GND | 100 | GND |
| 69 | Not connected | 85 | GND | 101 | GND |
| 70 | Not connected | 86 | GND | 102 | GND |
| 71 | Not connected | 87 | Not connected | 103 | GND |
| 72 | Not connected | 88 | GND | 104 | Not connected |
| 73 | Not connected | 89 | GND | 105 | Not connected |
| 74 | Do not use | 90 | GND | 106 | Not connected |
| 75 | Do not use | 91 | Not connected | 245 | GND |
| 76 | Do not use | 92 | GND | 246 | Not connected |
| 77 | Do not use | 93 | GND | 247 | Not connected |
| 78 | Do not use | 94 | GND | 248 | Not connected |
| 79 | Not connected | 95 | GND | 249 | Not connected |
| 80 | Do not use | 96 | GND | 250 | GND |
| 81 | GND | 97 | GND | 251 | GND |
| 82 | GND | 98 | GND | 252 | GND |

1. The MCLK signal is optionally configurable for GPIO4 or GPIO13.

Signal pads that are not used should not be connected to an external application.

Please note that the reference voltages listed in Table 2 are the values measured directly on the ELS61-E R2 module. They do not apply to the accessories connected.

## 2.1.2 Signal Properties

**Table 2:** Signal properties

| Function | Signal name | IO | Signal form and level | Comment |
|---|---|---|---|---|
| Power supply | $BATT+_{BB}$<br>$BATT+_{RF}$ | I | GSM activated:<br>$V_I$max = 4.5V<br>$V_I$norm = 3.8V<br>$V_I$min = 3.0V during Tx burst on board<br><br>I ≈ 2.3A, during Tx burst (GSM)<br><br>___\|¯¯¯¯¯\|_____\|¯¯¯¯¯\|___<br><br>n Tx = n x 577µs peak current every 4.616ms<br><br>WCDMA activated:<br>$V_I$max = 4.5V<br>$V_I$norm = 3.8V<br>$V_I$min = 3.0V during Transmit active.<br>Imax = 900mA during Tx<br><br>LTE activated:<br>$V_I$max = 4.5V<br>$V_I$norm = 3.8V<br>$V_I$min = 3.0V during Transmit active. | Lines of BATT+ and GND must be connected in parallel for supply purposes because higher peak currents may occur.<br><br>Minimum voltage must not fall below 3.0V including drop, ripple, spikes and not rise above 4.5V.<br><br>$BATT+_{BB}$ and $BATT+_{RF}$ require an ultra low ESR capacitor:<br>$BATT+_{BB}$ --> 150µF<br>$BATT+_{RF}$ --> 150µF<br>If using Multilayer Ceramic Chip Capacitors (MLCC) please take DC-bias into account.<br><br>Note that minimum ESR value is advised at <70mΩ. |
| Power supply | GND | | Ground | Application Ground |
| External supply voltage | V180 | O | Normal operation:<br>$V_O$norm = 1.80V ±3%<br>$I_O$max = -10mA<br><br>SLEEP mode Operation:<br>$V_O$Sleep = 1.80V ±5%<br>$I_O$max = -10mA<br><br>CLmax = 100µF | V180 should be used to supply level shifters at the interfaces or to supply external application circuits.<br><br>VCORE and V180 may be used for the power indication circuit.<br><br>**Vcore and V180 are sensitive against back-powering by other signals. While switched off these voltage domains must have <0.2V.**<br><br>If unused keep lines open. |
| | VCORE | O | $V_O$norm = 1.2V ±2.5%<br>$I_O$max = -10mA<br>CLmax = 100nF<br><br>SLEEP mode Operation:<br>$V_O$Sleep = 0.90V...1.2V ±4%<br>$I_O$max = -10mA | |
| Ignition | ON[1] | I | $V_{IH}$max = 5V tolerant<br>$V_{IH}$min = 1.3V<br>$V_{IL}$max = 0.5V<br>Slew rate ≤ 1ms<br><br>ON ___\|~~~~ | This signal switches the module on, and is rising edge sensitive triggered.<br><br>Internal pull down value for this signal is 100kΩ. |

**Table 2:** Signal properties

| Function | Signal name | IO | Signal form and level | Comment |
|---|---|---|---|---|
| Emergency restart | EMERG_RST | I | $R_I \approx 1k\Omega$, $C_I \approx 1nF$<br>$V_{OH}max$ = VDDLP max<br>$V_{IH}min$ = 1.35V<br>$V_{IL}max$ = 0.3V at ~200µA<br><br>~~\|___\|~~ low impulse width > 10ms | This line must be driven low by an open drain or open collector driver connected to GND.<br><br>If unused keep line open. |
| RTC backup | VDDLP | I/O | $V_O norm$ = 1.8V ±5%<br>$I_O max$ = -25mA<br><br>$V_I max$ = 1.9V<br>$V_I min$ = 1.0V<br>$I_I typ$ < 1µA | It is recommended to use a serial resistor between VDDLP and a possible capacitor (bigger than 1µF).<br><br>If unused keep line open. |
| USB | VUSB_IN | I | $V_I min$ = 3V<br>$V_I max$ = 5.25V<br><br>Active and suspend current:<br>$I_{max}$ < 100µA | All electrical characteristics according to USB Implementers' Forum, USB 2.0 Specification.<br><br>If unused keep lines open. |
| | USB_DN | I/O | Full and high speed signal characteristics according USB 2.0 Specification. | |
| | USB_DP | | | |
| Serial Interface ASC0 | RXD0 | O | $V_{OL}max$ = 0.25V at I = 1mA<br>$V_{OH}min$ = 1.55V at I = -1mA<br>$V_{OH}max$ = 1.85V | If unused keep lines open.<br><br>Note that some ASC0 lines are originally available as GPIO lines. If configured as ASC0 lines, the GPIO lines are assigned as follows:<br>GPIO1 --> DTR0<br>GPIO2 --> DCD0<br>GPIO3 --> DSR0<br>GPIO24 --> RING0<br><br>The DSR0 line is also shared with the SPI interface's SPI_CLK signal.<br><br>Note that DCD0/GPIO2 must not be driven low during startup |
| | CTS0 | O | | |
| | DSR0 | O | | |
| | DCD0 | O | | |
| | RING0 | O | | |
| | TXD0 | I | $V_{IL}max$ = 0.35V<br>$V_{IH}min$ = 1.30V<br>$V_{IH}max$ = 1.85V | |
| | RTS0 | I | Pull down resistor active<br>$V_{IL}max$ = 0.35V at > 50µA<br>$V_{IH}min$ = 1.30V at < 240µA<br>$V_{IH}max$ = 1.85V at < 240µA | |
| | DTR0 | I | Pull up resistor active<br>$V_{IL}max$ = 0.35V at < -200µA<br>$V_{IH}min$ = 1.30V at > -50µA<br>$V_{IH}max$ = 1.85V | |

**Table 2:** Signal properties

| Function | Signal name | IO | Signal form and level | Comment |
|---|---|---|---|---|
| Serial Interface ASC1 | RXD1 | O | $V_{OL}$max = 0.25V at I = 1mA<br>$V_{OH}$min = 1.55V at I = -1mA<br>$V_{OH}$max = 1.85V<br><br>$V_{IL}$max = 0.35V<br>$V_{IH}$min = 1.30V<br>$V_{IH}$max = 1.85V | If unused keep line open.<br><br>Note that the ASC1 interface lines are originally available as GPIO lines. If configured as ASC1 lines, the GPIO lines are assigned as follows:<br>GPIO16 --> RXD1<br>GPIO17 --> TXD1<br>GPIO18 --> RTS1<br>GPIO19 --> CTS1 |
| | TXD1 | I | | |
| | RTS1 | I | | |
| | CTS1 | O | | |
| SIM card detection | CCIN | I | $R_I$ ≈ 110kΩ<br>$V_{IH}$min = 1.45V at I = 15µA,<br>$V_{IH}$max= 1.9V<br>$V_{IL}$max = 0.3V | CCIN = High, SIM card inserted.<br><br>For details please refer to Section 2.1.6.<br><br>If unused keep line open. |
| 3V SIM Card Interface | CCRST | O | $V_{OL}$max = 0.30V at I = 1mA<br>$V_{OH}$min = 2.45V at I = -1mA<br>$V_{OH}$max = 2.90V | Maximum cable length or copper track to SIM card holder should not exceed 100mm. |
| | CCIO | I/O | $V_{IL}$max = 0.50V<br>$V_{IH}$min = 2.05V<br>$V_{IH}$max = 2.90V<br><br>$V_{OL}$max = 0.25V at I = 1mA<br>$V_{OH}$min = 2.50V at I = -1mA<br>$V_{OH}$max = 2.90V | |
| | CCCLK | O | $V_{OL}$max = 0.25V at I = 1mA<br>$V_{OH}$min = 2.40V at I = -1mA<br>$V_{OH}$max = 2.90V | |
| | CCVCC | O | $V_O$min= 2.70V<br>$V_O$typ = 2.90V<br>$V_O$max = 3.30V<br>$I_O$max = -30mA | |

**Table 2:** Signal properties

| Function | Signal name | IO | Signal form and level | Comment |
|---|---|---|---|---|
| 1.8V SIM Card Interface | CCRST | O | $V_{OL}$max = 0.25V at I = 1mA<br>$V_{OH}$min = 1.45V at I = -1mA<br>$V_{OH}$max = 1.90V | Maximum cable length or copper track to SIM card holder should not exceed 100mm. |
| | CCIO | I/O | $V_{IL}$max = 0.35V<br>$V_{IH}$min = 1.25V<br>$V_{IH}$max = 1.85V<br><br>$V_{OL}$max = 0.25V at I = 1mA<br>$V_{OH}$min = 1.50V at I = -1mA<br>$V_{OH}$max = 1.85V | |
| | CCCLK | O | $V_{OL}$max = 0.25V at I = 1mA<br>$V_{OH}$min = 1.50V at I = -1mA<br>$V_{OH}$max = 1.85V | |
| | CCVCC | O | $V_O$min = 1.75V<br>$V_O$typ = 1.80V<br>$V_O$max = 1.85V<br>$I_O$max = -30mA | |
| $I^2C$ | I2CCLK | IO | Open drain IO<br>$V_{OL}$min = 0.35V at Imax = 4mA (Imax = Imax external + I pull-up)<br>$V_{OH}$max = 1.85V<br>R external pull up min = 560Ω<br><br>$V_{IL}$max = 0.35V<br>$V_{IH}$min = 1.3V<br>$V_{IH}$max = 1.85V | According to the $I^2C$ Bus Specification Version 2.1 for the fast mode a rise time of max. 300ns is permitted. There is also a maximum $V_{OL}$=0.4V at 3mA specified.<br><br>The value of the pull-up depends on the capacitive load of the whole system ($I^2C$ Slave + lines). The maximum sink current of I2CDAT and I2CCLK is 4mA.<br><br>$I^2C$ interface of the module already has internal 1KOhm pull up resistor to V180 inside the module. Please take this into consideration during application design.<br><br>If lines are unused keep lines open. |
| | I2CDAT | IO | | |

**Table 2:** Signal properties

| Function | Signal name | IO | Signal form and level | Comment |
|---|---|---|---|---|
| SPI | SPI_CLK | O | $V_{OL}$max = 0.25V at I = 1mA<br>$V_{OH}$min = 1.55V at I = -1mA<br>$V_{OH}$max = 1.85V<br><br>$V_{IL}$max = 0.35V<br>$V_{IH}$min = 1.30V<br>$V_{IH}$max = 1.85V | If lines are unused keep lines open.<br><br>Note that the SPI interface lines are originally available as GPIO lines. If configured as SPI lines, the GPIO lines are assigned as follows:<br>GPIO3 --> SPI_CLK<br>GPIO16 --> MOSI<br>GPIO17 --> MISO<br>GPIO19 --> SPI_CS |
| | MOSI | O | | |
| | MISO | I | | |
| | SPI_CS | O | | |
| GPIO interface | GPIO1-GPIO3 | IO | $V_{OL}$max = 0.25V at I = 1mA<br>$V_{OH}$min = 1.55V at I = -1mA<br>$V_{OH}$max = 1.85V<br><br>$V_{IL}$max = 0.35V<br>$V_{IH}$min = 1.30V<br>$V_{IH}$max = 1.85V<br><br>Imax = ±5mA | If unused keep line open.<br><br>Please note that most GPIO lines can be configured by AT command for alternative functions:<br>GPIO1-GPIO3: ASC0 control lines DTR0, DCD0 and DSR0<br>GPIO4: Fast shutdown, MCLK[2]<br>GPIO5: Status LED line<br>GPIO6/GPIO7: PWM<br>GPIO8: Pulse Counter<br>GPIO13: MCLK[2]<br>GPIO16-GPIO19: ASC1 or SPI<br>GPIO20-GPIO23: DAI<br>GPIO24: ASC0 control line RING0 |
| | GPIO4 | IO | | |
| | GPIO5 | IO | | |
| | GPIO6 | IO | | |
| | GPIO7 | IO | | |
| | GPIO8 | IO | | |
| | GPIO11-GPIO15 | IO | | |
| | GPIO16-GPIO19 | IO | | |
| | GPIO20-GPIO23 | IO | | |
| | GPIO24 | IO | | |
| Fast shutdown | FST_SHDN | I | $V_{IL}$max = 0.35V<br>$V_{IH}$min = 1.30V<br>$V_{IH}$max = 1.85V<br><br>~~\|___\|~~ low impulse width > 1ms | This line must be driven low.<br>If unused keep line open.<br><br>Note that the fast shutdown line is originally available as GPIO line. If configured as fast shutdown, the GPIO line is assigned as follows:<br>GPIO4 --> FST_SHDN |
| Status LED | LED | O | $V_{OL}$max = 0.25V at I = 1mA<br>$V_{OH}$min = 1.55V at I = -1mA<br>$V_{OH}$max = 1.85V | If unused keep line open.<br><br>Note that the LED line is originally available as GPIO line. If configured as LED line, the GPIO line is assigned as follows:<br>GPIO5 --> LED |

**Table 2:** Signal properties

| Function | Signal name | IO | Signal form and level | Comment |
|---|---|---|---|---|
| PWM | PWM1 | O | $V_{OL}$max = 0.25V at I = 1mA<br>$V_{OH}$min = 1.55V at I = -1mA<br>$V_{OH}$max = 1.85V | If unused keep lines open.<br><br>Note that the PWM lines are originally available as GPIO lines. If configured as PWM lines, the GPIO lines are assigned as follows:<br>GPIO7 --> PWM1<br>GPIO6 --> PWM2 |
| | PWM2 | O | | |
| Pulse counter | COUNTER | I | Internal up resistor active<br>$V_{IL}$max = 0.35V at < -200µA<br>$V_{IH}$min = 1.30V at > -50µA<br>$V_{IH}$max = 1.85V | If unused keep line open.<br><br>Note that the COUNTER line is originally available as GPIO line. If configured as COUNTER line, the GPIO line is assigned as follows:<br>GPIO8 --> COUNTER |
| Digital audio interface (DAI) | FSC | O | $V_{OL}$max = 0.25V at I = 1mA<br>$V_{OH}$min = 1.55V at I = -1mA<br>$V_{OH}$max = 1.85V | If unused keep line open.<br><br>Note that the DAI interface lines are originally available as GPIO lines. If configured as DAI lines, the GPIO lines are assigned as follows:<br>GPIO22 --> FSC<br>GPIO23 --> BCLK<br>GPIO20 --> DOUT<br>GPIO21 --> DIN<br>GPIO4 or GPIO13 --> MCLK (Master clock out for external codecs) |
| | BCLK | O | | |
| | DOUT | O | | |
| | DIN | I | $V_{IL}$max = 0.35V<br>$V_{IH}$min = 1.30V<br>$V_{IH}$max = 1.85V | |
| | MCLK | O | $V_{OL}$max = 0.25V at I = 1mA<br>$V_{OH}$min = 1.55V at I = -1mA<br>$V_{OH}$max = 1.85V<br>f=13MHz | |
| ADC (Analog-to-Digital Converter) | ADC1 | I | $R_I$ = 1MΩ<br>$V_I$ = 0V ... 1.2V (valid range)<br>$V_{IH}$ max = 1.2V<br><br>Resolution 1024 steps<br>Tolerance 0.3% | ADC can be used as input for external measurements.<br><br>If unused keep line open. |

1. After the operating voltage is applied, it is required to wait at least 1 second to trigger the ON signal.
2. The MCLK signal is optionally configurable for GPIO4 or GPIO13.

#### 2.1.2.1 Absolute Maximum Ratings

The absolute maximum ratings stated in Table 3 are stress ratings under any conditions. Stresses beyond any of these limits will cause permanent damage to ELS61-E R2.

**Table 3:** Absolute maximum ratings[1]

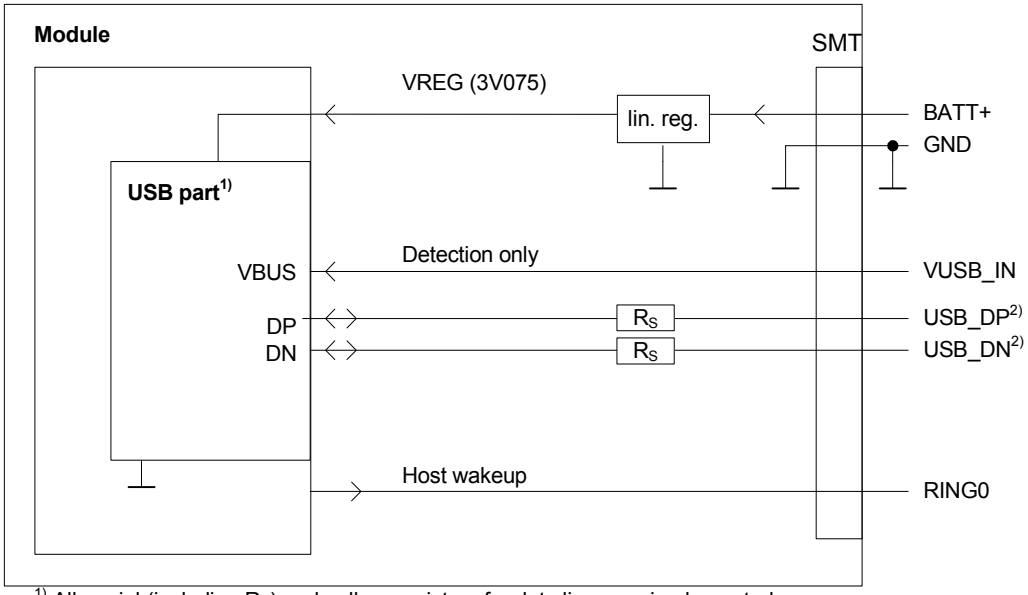
| Parameter | Min | Max | Unit |
|---|---|---|---|
| Supply voltage $BATT+_{BB}$, $BATT+_{RF}$ | -0.5 | +5.5 | V |
| Voltage at all signal lines in Power Down mode | -0.3 | +0.3 | V |
| Voltage at digital lines in normal operation | -0.2 | V180 + 0.2 | V |
| Voltage at SIM/USIM interface, CCVCC in normal operation | -0.5 | +3.3 | V |
| VDDLP input voltage | -0.15 | 2.0 | V |
| Voltage at ADC line in normal operation | 0 | 1.2 | V |
| V180 in normal operation | +1.7 | +1.9 | V |
| Current at V180 in normal operation | -0 | +50 | mA |
| VCORE in normal operation | +0.85 | +1.25 | V |
| Current at VCORE in normal operation | -0 | +50 | mA |
| Voltage at ON signal | -0.5 | +6.5 | V |
| Current at single GPIO | -5 | +5 | mA |
| Current at all GPIO | -50 | +50 | mA |
| Voltage at VCORE, V180 in power down mode | -0.2 | +0.2 | V |

1. Positive noted current means current sourcing from ELS61-E R2. Negative noted current means current sourcing towards ELS61-E R2.

## 2.1.3 USB Interface

ELS61-E R2 supports a USB 2.0 High Speed (480Mbit/s) device interface that is Full Speed (12Mbit/s) compliant. The USB interface is primarily intended for use as command and data interface and for downloading firmware.

The external application is responsible for supplying the VUSB_IN line. This line is used for cable detection only. The USB part (driver and transceiver) is supplied by means of BATT+. This is because ELS61-E R2 is designed as a self-powered device compliant with the “Universal Serial Bus Specification Revision 2.0”[1].




1) All serial (including $R_S$) and pull-up resistors for data lines are implemented.
2) If the USB interface is operated in High Speed mode (480MHz), it is recommended to take special care routing the data lines USB_DP and USB_DN. Application layout should in this case implement a differential impedance of 90 ohms for proper signal integrity.

**Figure 5:** USB circuit

To properly connect the module's USB interface to the external application, a USB 2.0 compatible connector and cable or hardware design is required. For more information on the USB related signals see Table 2. Furthermore, the USB modem driver distributed with ELS61-E R2 needs to be installed.

1. The specification is ready for download on http://www.usb.org/developers/docs/

### 2.1.3.1 Reducing Power Consumption

While a USB connection is active, the module will never switch into SLEEP mode. Only if the USB interface is in Suspended state or Detached (i.e., VUSB_IN = 0) is the module able to switch into SLEEP mode thereby saving power. There are two possibilities to enable power reduction mechanisms:

- **Recommended implementation of USB Suspend/Resume/Remote Wakeup:**
  The USB host should be able to bring its USB interface into the Suspended state as described in the “Universal Serial Bus Specification Revision 2.0“[1]. For this functionality to work, the VUSB_IN line should always be kept enabled. On incoming calls and other events ELS61-E R2 will then generate a Remote Wakeup request to resume the USB host controller.

  See also [6] (USB Specification Revision 2.0, Section 10.2.7, p.282):
  "If USB System wishes to place the bus in the Suspended state, it commands the Host Controller to stop all bus traffic, including SOFs. This causes all USB devices to enter the Suspended state. In this state, the USB System may enable the Host Controller to respond to bus wakeup events. This allows the Host Controller to respond to bus wakeup signaling to restart the host system."

- **Implementation for legacy USB applications not supporting USB Suspend/Resume:**
  As an alternative to the regular USB suspend and resume mechanism it is possible to employ the RING0 line to wake up the host application in case of incoming calls or events signalized by URCs while the USB interface is in Detached state (i.e., VUSB_IN = 0). Every wakeup event will force a new USB enumeration. Therefore, the external application has to carefully consider the enumeration timings to avoid loosing any signalled events. For details on this host wakeup functionality see Section 2.1.14.3. To prevent existing data call connections from being disconnected while the USB interface is in detached state (i.e., VUSB_IN=0) it is possible to call AT&D0, thus ignoring the status of the DTR line (see also [1]).

1. The specification is ready for download on http://www.usb.org/developers/docs/

### 2.1.4 Serial Interface ASC0

ELS61-E R2 offers an 8-wire unbalanced, asynchronous modem interface ASC0 conforming to ITU-T V.24 protocol DCE signaling. The electrical characteristics do not comply with ITU-T V.28. The significant levels are 0V (for low data bit or active state) and 1.8V (for high data bit or inactive state). For electrical characteristics please refer to Table 2. For an illustration of the interface line's startup behavior see Figure 7.

ELS61-E R2 is designed for use as a DCE. Based on the conventions for DCE-DTE connections it communicates with the customer application (DTE) using the following signals:
- Port TXD @ application sends data to the module's TXD0 signal line
- Port RXD @ application receives data from the module's RXD0 signal line

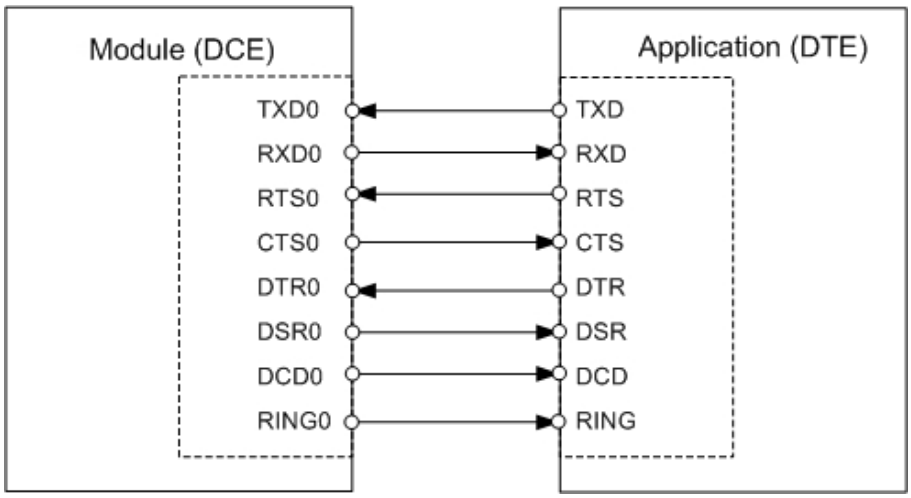
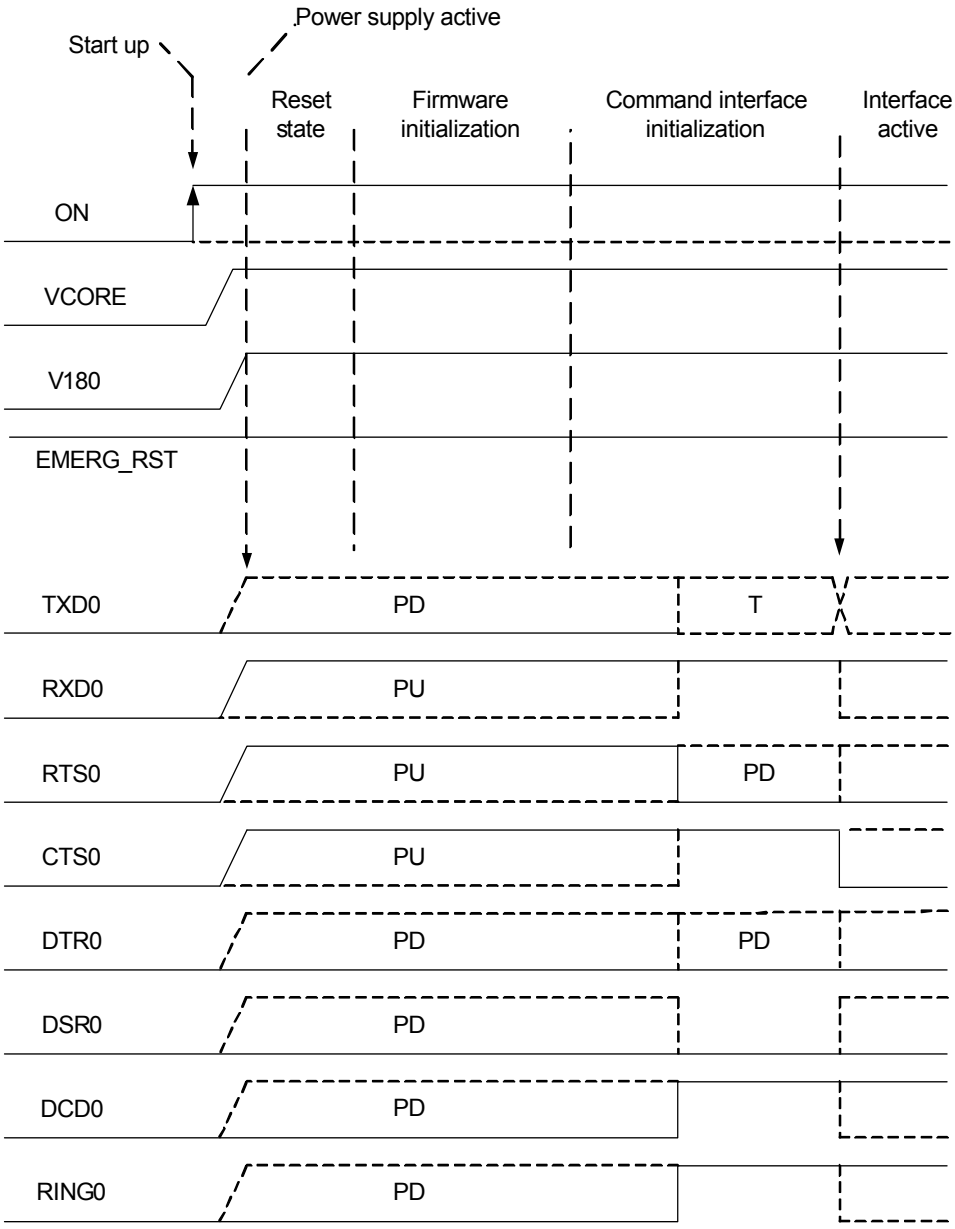



**Figure 6:** Serial interface ASC0

Features:
- Includes the data lines TXD0 and RXD0, the status lines RTS0 and CTS0 and, in addition, the modem control lines DTR0, DSR0, DCD0 and RING0.
- The RING0 signal serves to indicate incoming calls and other types of URCs (Unsolicited Result Code). It can also be used to send pulses to the host application, for example to wake up the application from power saving state.
- Configured for 8 data bits, no parity and 1 stop bit.
- ASC0 can be operated at fixed bit rates from 1,200bps up to 3Mbps.
- Autobauding supports bit rates from 1,200bps up to 230,400bps.
- Supports RTS0/CTS0 hardware flow control. The hardware hand shake line RTS0 has an internal pull down resistor causing a low level signal, if the line is not used and open. Although hardware flow control is recommended, this allows communication by using only RXD and TXD lines.
- Wake up from SLEEP mode by RTS0 activation (high to low transition; see Section 3.4.3).

Note: The ASC0 modem control lines DTR0, DCD0, DSR0 and RING0 are originally available as GPIO lines. If configured as ASC0 lines, these GPIO lines are assigned as follows: GPIO1 --> DTR0, GPIO2 --> DCD0, GPIO3 --> DSR0 and GPIO24 --> RING0. Also, DSR0 is shared with the SPI_CLK line of the SPI interface and may be configured as such. Configuration is done by AT command (see [1]). The configuration is non-volatile and becomes active after a module restart.

The following figure shows the startup behavior of the asynchronous serial interface ASC0.




For pull-up and pull-down values see Table 15.

**Figure 7:** ASC0 startup behavior

Notes:
During startup the DTR0 signal is driven active low for 500µs. It is recommended to provide a 470Ω serial resistor for the DTR0 line to prevent shorts (high current flow).

No data must be sent over the ASC0 interface before the interface is active and ready to receive data (see Section 3.2.1).

An external pull down to ground on the DCD0 line during the startup phase activates a special mode for ELS61-E R2. In this special mode the AT command interface is not available and the module may therefore no longer behave as expected.

### 2.1.5 Serial Interface ASC1

Four ELS61-E R2 GPIO lines can be configured as ASC1 interface signals to provide a 4-wire unbalanced, asynchronous modem interface ASC1 conforming to ITU-T V.24 protocol DCE signaling. The electrical characteristics do not comply with ITU-T V.28. The significant levels are 0V (for low data bit or active state) and 1.8V (for high data bit or inactive state). For electrical characteristics please refer to Table 2. For an illustration of the interface line's startup behavior see Figure 9.

The ASC1 interface lines are originally available as GPIO lines. If configured as ASC1 lines, the GPIO lines are assigned as follows: GPIO16 --> RXD1, GPIO17 --> TXD1, GPIO18 --> RTS1 and GPIO19 --> CTS1. Configuration is done by AT command (see [1]: AT^SCFG). The configuration is non-volatile and becomes active after a module restart.

ELS61-E R2 is designed for use as a DCE. Based on the conventions for DCE-DTE connections it communicates with the customer application (DTE) using the following signals:
- Port TXD @ application sends data to module's TXD1 signal line
- Port RXD @ application receives data from the module's RXD1 signal line

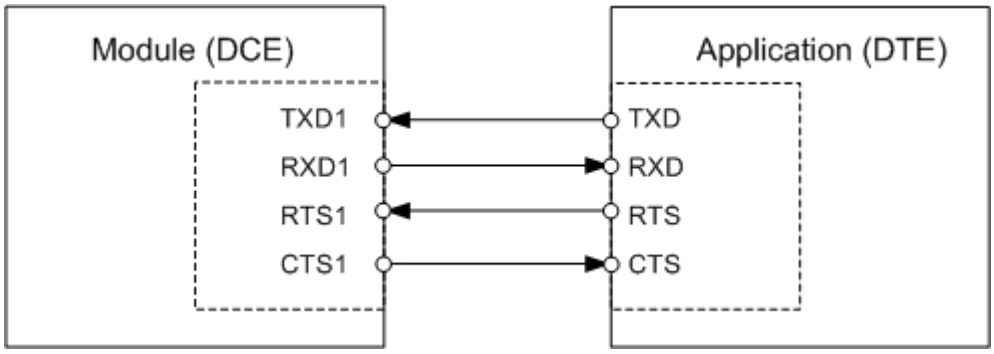
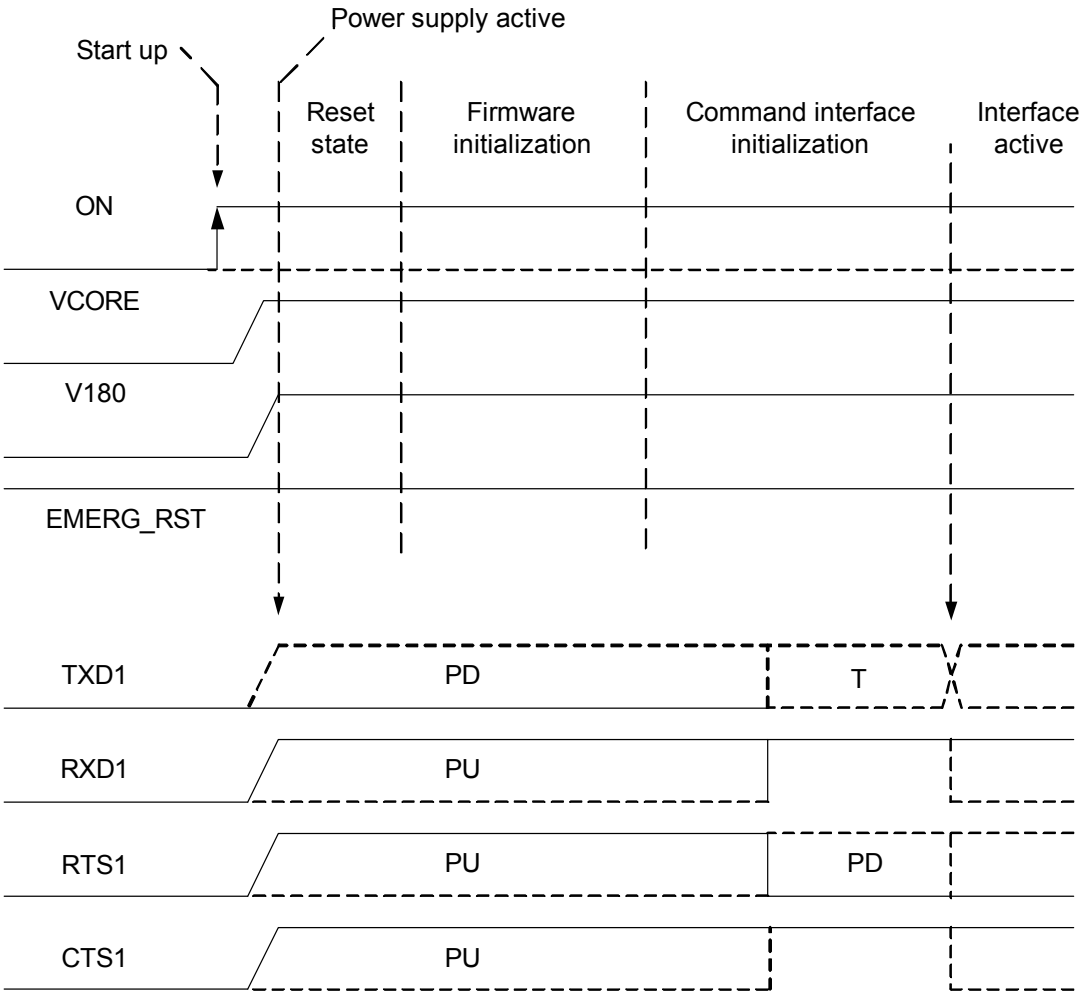



**Figure 8:** Serial interface ASC1

Features
- Includes only the data lines TXD1 and RXD1 plus RTS1 and CTS1 for hardware handshake.
- On ASC1 no RING line is available.
- Configured for 8 data bits, no parity and 1 or 2 stop bits.
- ASC1 can be operated at fixed bit rates from 1,200 bps to 921,600 bps.
- Autobauding supports bit rates from 1,200bps up to 230,400bps.
- Supports RTS1/CTS1 hardware flow. The hardware hand shake line RTS0 has an internal pull down resistor causing a low level signal, if the line is not used and open. Although hardware flow control is recommended, this allows communication by using only RXD and TXD lines.

The following figure shows the startup behavior of the asynchronous serial interface ASC1.




*) For pull-down values see Table 15.

**Figure 9:** ASC1 startup behavior

### 2.1.6 UICC/SIM/USIM Interface

ELS61-E R2 has an integrated UICC/SIM/USIM interface compatible with the 3GPP 31.102 and ETSI 102 221. This is wired to the host interface in order to be connected to an external SIM card holder. Five pads on the SMT application interface are reserved for the SIM interface.

The UICC/SIM/USIM interface supports 3V and 1.8V SIM cards. Please refer to Table 2 for electrical specifications of the UICC/SIM/USIM interface lines depending on whether a 3V or 1.8V SIM card is used.

The CCIN signal serves to detect whether a tray (with SIM card) is present in the card holder. Using the CCIN signal is mandatory for compliance with the GSM 11.11 recommendation if the mechanical design of the host application allows the user to remove the SIM card during operation. To take advantage of this feature, an appropriate SIM card detect switch is required on the card holder. For example, this is true for the model supplied by Molex, which has been tested to operate with ELS61-E R2 and is part of the Thales reference equipment submitted for type approval. See Section 7.1 for Molex ordering numbers.

**Table 4:** Signals of the SIM interface (SMT application interface)

| Signal | Description |
|---|---|
| GND | Separate ground connection for SIM card to improve EMC. |
| CCCLK | Chipcard clock |
| CCVCC | SIM supply voltage. |
| CCIO | Serial data line, input and output. |
| CCRST | Chipcard reset |
| CCIN | Input on the baseband processor for detecting a SIM card tray in the holder. If the SIM is removed during operation the SIM interface is shut down immediately to prevent destruction of the SIM. The CCIN signal is by default low and will change to high level if a SIM card is inserted.<br>The CCIN signal is mandatory for applications that allow the user to remove the SIM card during operation.<br>The CCIN signal is solely intended for use with a SIM card. It must not be used for any other purposes. Failure to comply with this requirement may invalidate the type approval of ELS61-E R2. |

Note [1]: No guarantee can be given, nor any liability accepted, if loss of data is encountered after removing the SIM card during operation. Also, no guarantee can be given for properly initializing any SIM card that the user inserts after having removed the SIM card during operation. In this case, the application must restart ELS61-E R2.

Note [2]: On the evaluation board, the CCIN signal is inverted, thus the CCIN signal is by default high and will change to a low level if a SIM card is inserted.

The figure below shows a circuit to connect an external SIM card holder.

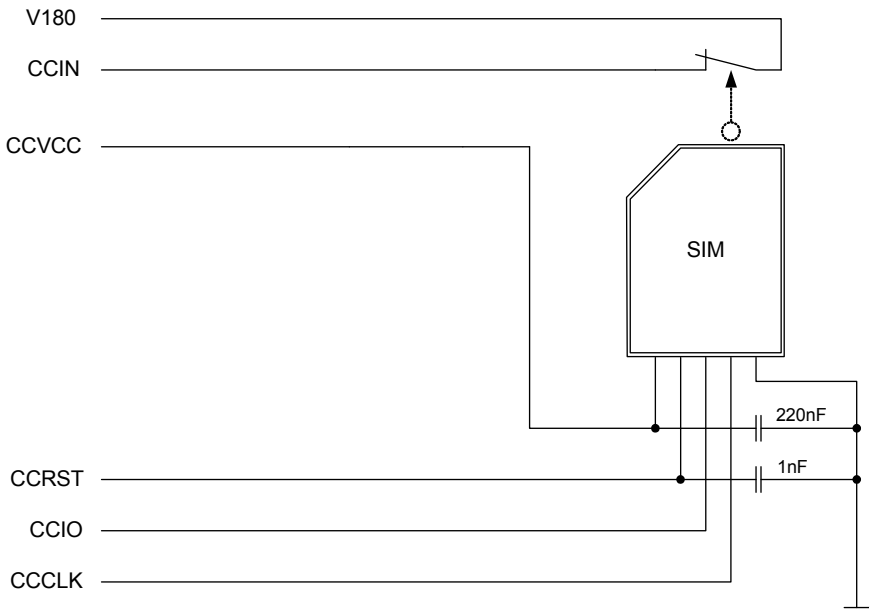



**Figure 10:** External UICC/SIM/USIM card holder circuit

The total cable length between the SMT application interface pads on ELS61-E R2 and the pads of the external SIM card holder must not exceed 100mm in order to meet the specifications of 3GPP TS 51.010-1 and to satisfy the requirements of EMC compliance.

To avoid possible cross-talk from the CCCLK signal to the CCIO signal be careful that both lines are not placed closely next to each other. A useful approach is using a GND line to shield the CCIO line from the CCCLK line.

An example for an optimized ESD protection for the SIM interface is shown in Section 2.1.6.1.

### 2.1.6.1 Enhanced ESD Protection for SIM Interface

To optimize ESD protection for the SIM interface it is possible to add ESD diodes to the SIM interface lines as shown in the example given in Figure 11.[1]

The example was designed to meet ESD protection according ETSI EN 301 489-1/52: Contact discharge: ± 4kV, air discharge: ± 8kV.

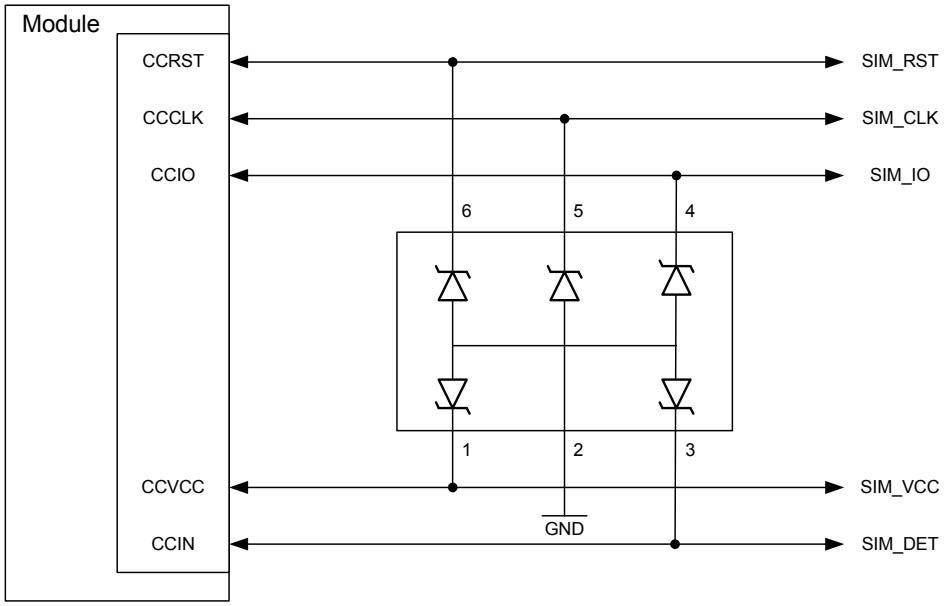



**Figure 11:** SIM interface - enhanced ESD protection

1. Note that the protection diode shall have low internal capacitance less than 5pF for IO and CLK.

### 2.1.7 Digital Audio Interface (DAI)

ELS61-E R2 supports a digital audio interface that can be employed either as pulse code modulation interface (see Section 2.1.7.1) or as inter IC sound interface (see Section 2.1.7.2). Operation of these interface variants is mutually exclusive, and can be configured by AT command (AT^SAIC; see [1]).

#### 2.1.7.1 Pulse Code Modulation Interface (PCM)

Four ELS61-E R2 GPIO lines can be configured as pule code modulation interface (PCM). The PCM functionality allows for the use of an external codec like the W681360 (see Section 2.1.7.3).

The PCM interface supports the following features:
- Master and Slave mode
- Long frame and short frame
- 8kHz sample rate / 125µs frame duration (narrow band), 16kHz sample rate / 62.5µs frame duration (wide band)
- Bit clock: 256kHz (PCM long frame, sample rate: 8kHz), 264kHz (PCM short frame, sample rate: 8kHz), 512kHz (PCM long frame, sample rate: 16kHz), 528kHz (PCM short frame, sample rate: 16kHz)
- The most significant bit MSB is transferred first
- Data write at rising edge / data read at falling edge
- Common frame sync signal for transmit and receive

The four GPIO lines can be configured as DAI/PCM interface signals as follows: GPIO20 --> DOUT, GPIO21--> DIN, GPIO22 --> FSC and GPIO23 --> BCLK. The configuration is done by AT command (see [1]). It is non-volatile and becomes active after a module restart. Table 5 describes the available DAI/PCM lines at the digital audio interface. For electrical details see Section 2.1.2.

**Table 5:** Overview of DAI/PCM lines

| Signal name | Input/Output | Description |
|---|---|---|
| DOUT | O | PCM data from ELS61-E R2 to external codec. |
| DIN | I | PCM data from external codec to ELS61-E R2. |
| FSC | O | Frame synchronization signal to external codec: Long frame (8kHz/16kHz) |
| BCLK | O | Bit clock to external codec. |
| MCLK | O | Optional master clock out to supply external codec. |

Figure 12 shows the PCM timing for the master mode available with ELS61-E R2.

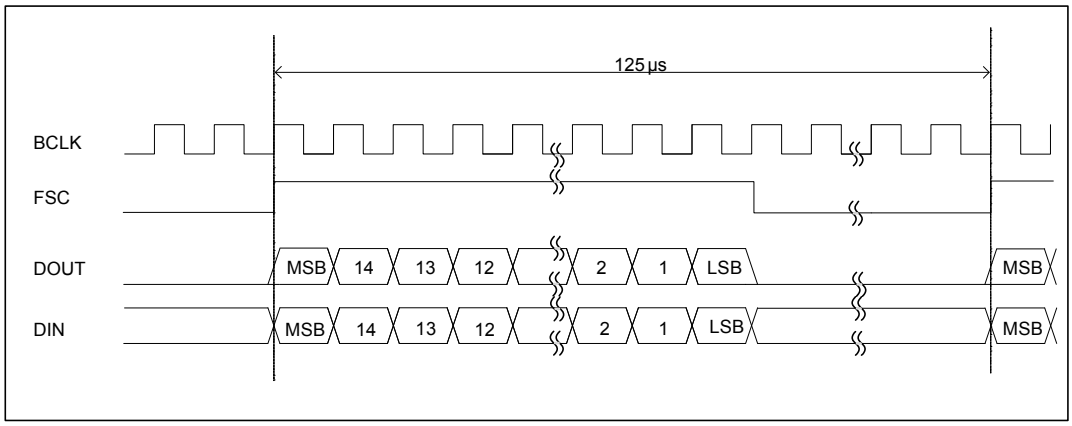



**Figure 12:** Long frame PCM timing, 256kHz

The following figure shows the start up behavior of the DAI interface. The start up configuration of functions will be activated after the software initialization of the command interface. With an active state of CTS0 (low level) the initialization of the DAI interface is finished.

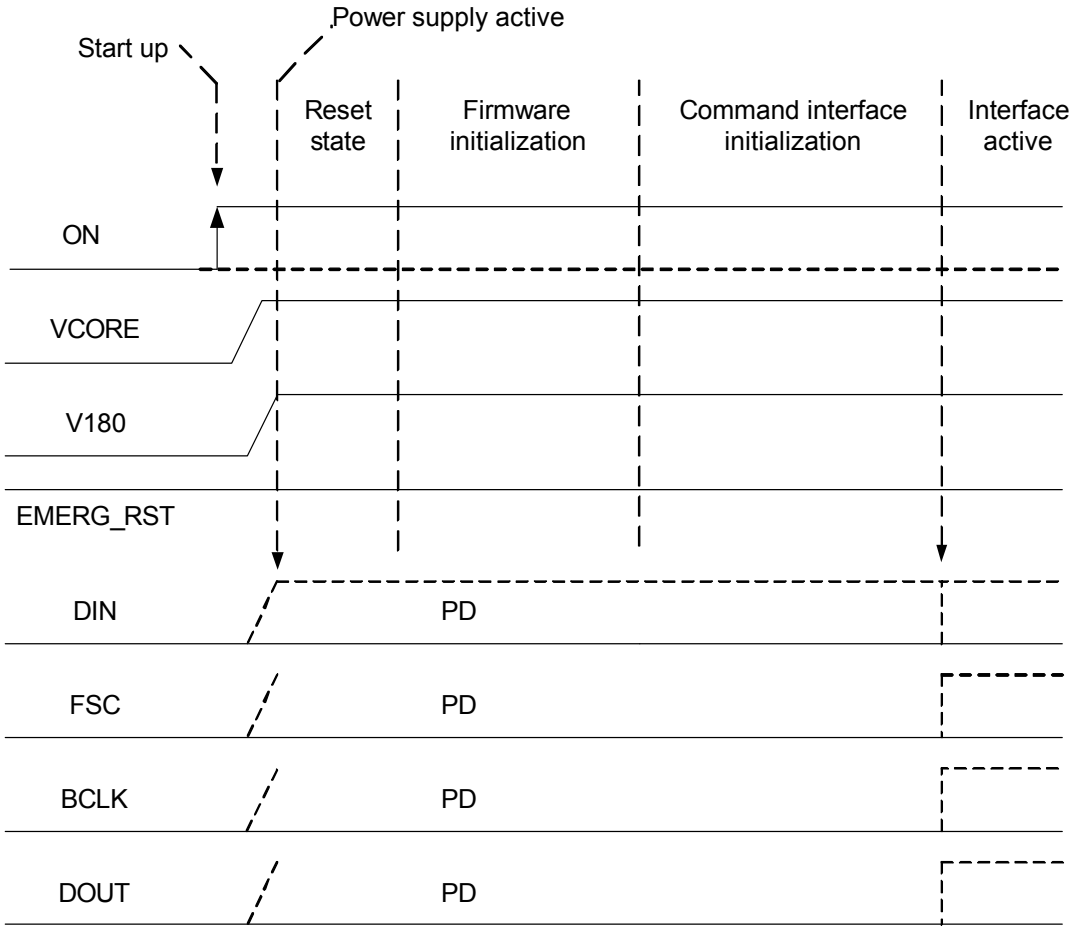



**Figure 13:** DAI startup timing

### 2.1.7.2 Inter IC Sound Interface

The Inter IC Sound interface ($I^2S$) is enabled using the AT command AT^SAIC (see [1]). An activation is possible only out of call and out of tone presentation. The $I^2S$ properties and capabilities comply with the requirements laid out in the Phillips $I^2S$ Bus Specifications, revised June 5, 1996.

The $I^2S$ interface has the following characteristics:

- Clock Modes: Master with permanent clock option
- Sampling Rate: 8kHz (narrow band), 16kHz (wide band)
- Bit clock: 256kHz (sample rate: 8kHz), 512kHz (sample rate: 16kHz)

The digital audio interface pads available for the PCM interface are also available for the $I^2S$ interface. In $I^2S$ mode they have the same electrical characteristics (for more information on the DOUT, DIN, FSC, and BCLK pads please refer to Section 2.1.2 and Section 2.1.7.1).

The table below lists the available pads at the module's digital audio interface.

**Table 6:** Overview of DAI/$I^2S$ lines

| Signal name | Input/Output | Description |
|---|---|---|
| DOUT | O | $I^2S$ data from module to external codec. |
| DIN | I | $I^2S$ data from external codec to module. |
| FSC | O | Frame synchronization signal to external codec: Word alignment (WS) |
| BCLK | O | Bit clock to external codec: 256kHz/512kHz |
| MCLK | O | Optional master clock out to supply external codecs. |

The following figure shows the $I^2S$ timing for the master mode available with the module.

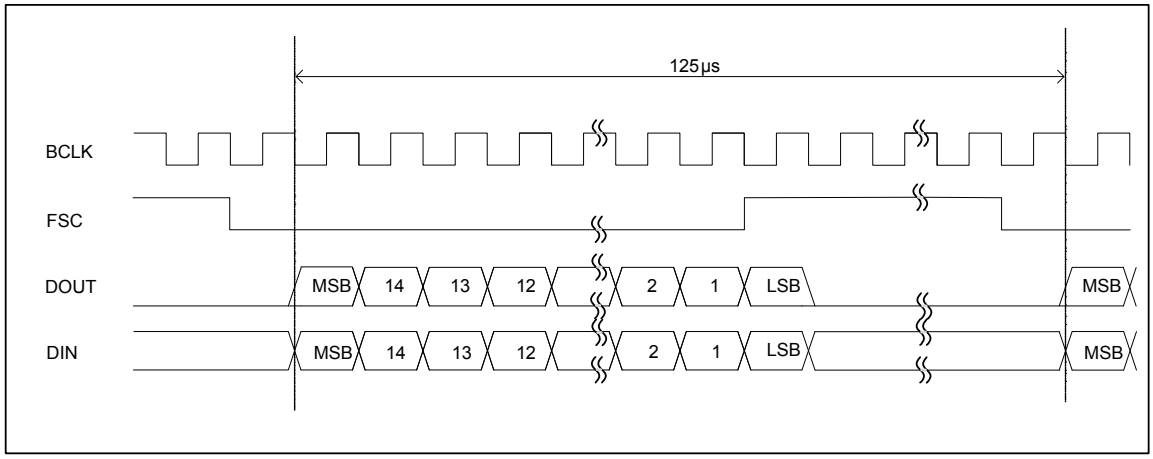



**Figure 14:** $I^2S$ timing, 8kHz sample rate

### 2.1.7.3 Solutions for the Digital Audio Interface

There are three examples of using the digital audio interface of the module below.

First of those samples is Nuvoton codec W681360 which can be replaced with a DSP. In the example, framesync (FSC) and clock (BCLK) master is the module. Thus the slave mode codec chip runs synchronously to the network.

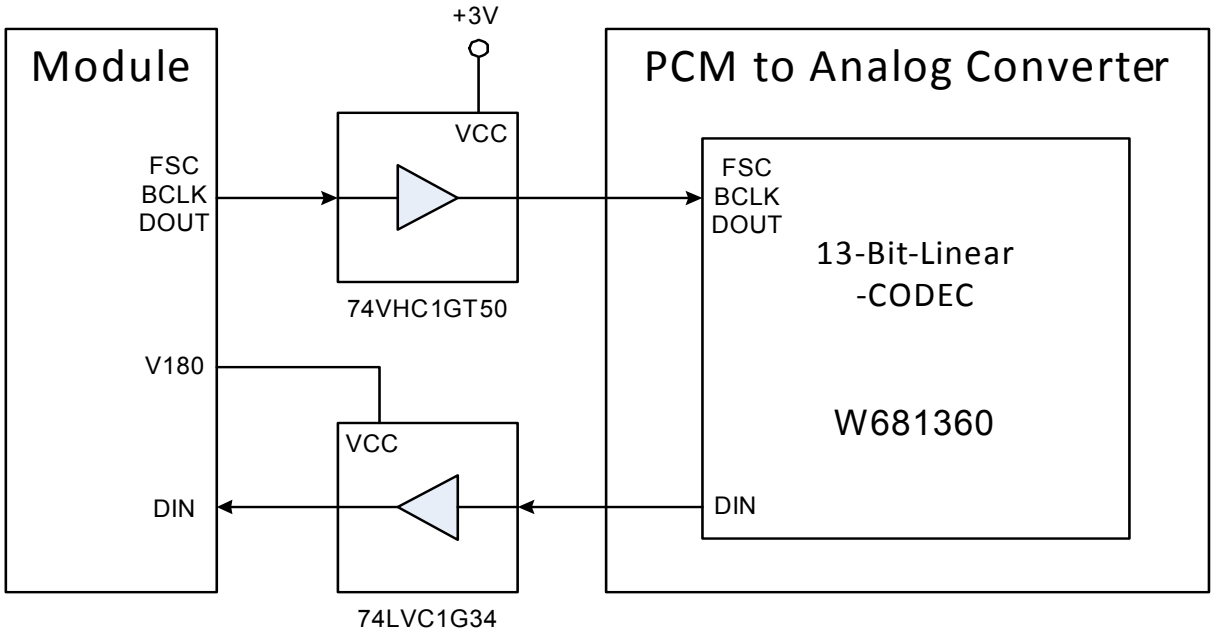



**Figure 15:** Block circuit connection for module's DAI interface to codec chip W681360

The Wolfson WM8944B is the second sample and needs to be controlled via I²C interface. V180 is used for its digital core supply and does not need level shifter for the digital audio interface. In the below figure, module is set to master for the framesync and the clock.

If module works in master I²S mode, this can be done via the following AT command:
AT^SAIC=3,"","","",0,0,1,0,0

Correspondingly, the related codec register settings are presented below:

**Table 7:** Codec register settings

| Register | Setting |
|---|---|
| Audio interface | R4(04h)=0x0002 |
| Compounding control | R5(05h)=0x0000 |
| Clock Gen control | R6(06h)=0x0340 |
| Additional control | R7(07h)=0x8013 |
| FLL Control1 | R8(08h)=0x0709 |
| FLL Control2 | R9(09h)=0x0000 |
| FLL Control3 | R10(Ah)=0x0C00 |

The module can also work as slave via AT^SAIC. At the same time, codec chipset needs to be set to master.

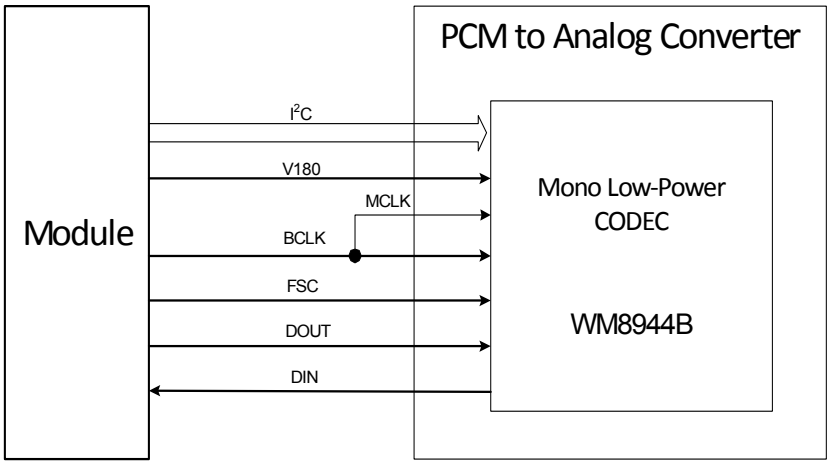



**Figure 16:** Block circuit connection for module's DAI interface to codec chip WM8944B

The Nuvoton NAU8814 codec is the third example and it needs to be controlled via $I^2C$ interface. What is more, an external 10MHz to 20MHz MCLK is needed.

Please note that the module's GPIO4 or GPIO13 lines may optionally be configured as MCLK output (13MHz clock). The configuration is done by AT command (see [1]). It is non-volatile and becomes active after a module restart.

V180 is used for its digital core supply and the level shifter is not needed for the digital audio interface. In the figure presented below, the module is the master for the framesync and the clock.

The module is set to a master and PCM long frame mode by default and it is recommended, to use it as shown below:
AT^SAIC=1,"","","",0,0,1,0,0

Correspondingly, the related codec register settings are at MCLK=13MHz condition.

**Table 8:** Codec register settings for MCLK=13MHz

| Register | Setting |
|---|---|
| Audio Interface Control | NAUregister[ 4] = 0x198 |
| Audio Interface Companding Control | NAUregister[ 5] = 0x000 |
| Clock Control | NAUregister[ 6] =0X1E0 |
| Audio Sample Rate Control | NAUregister[ 7] = 0x00A |
| PLL Control | NAUregister[ 0x24]=0x007 |
| | NAUregister[ 0x25]=0x023 |
| | NAUregister[ 0x26]=0x1EA |
| | NAUregister[ 0x27]=0x091 |

The module can also work as a slave via the AT^SAIC command and at the same time, the codec's chipset has to be set as a master.

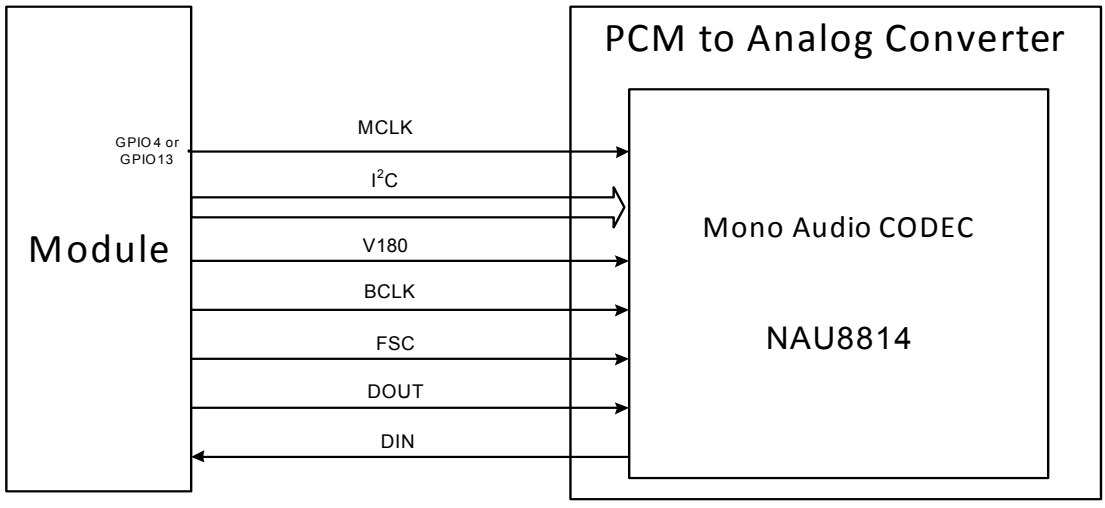



**Figure 17:** Block circuit connection of module DAI interface to codec chip NAU8814

Please note that different vendors may use different names for $I^2S$ interface signals in their datasheet, e.g., FS, WS and LRCLK are all commonly used for synchronization signals, SCLK and BCLK are commonly used for clock signals.

The below sample of a DAI analog converter for the Nouvoton codec W681360 is well suited for evaluating and testing a telephone handset and can be used instead of the headset interface of the DSB75.

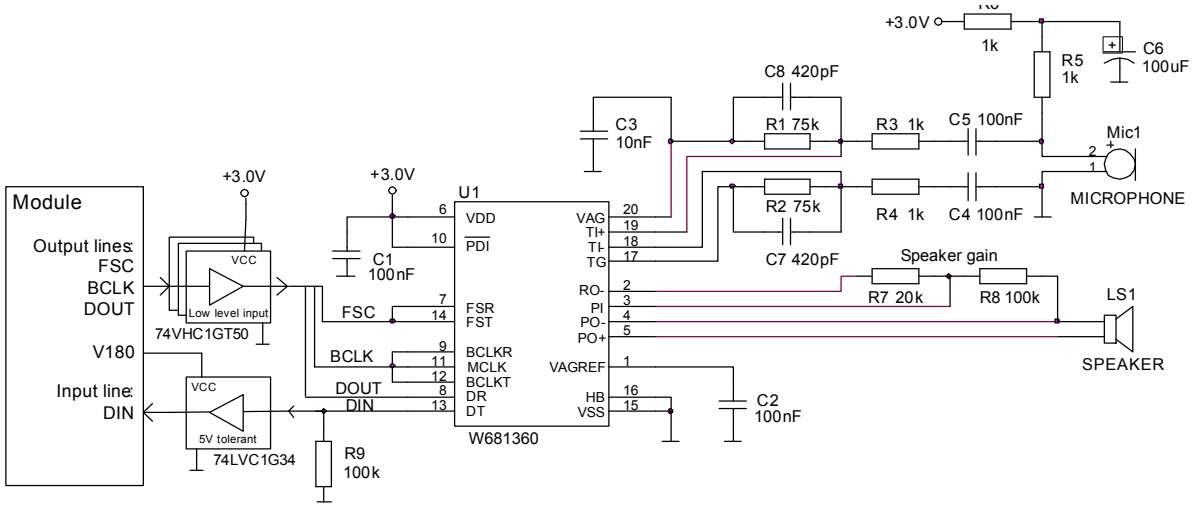



**Figure 18:** Sample circuit for analog to DAI box

The DAI interface has to be enabled. This can be done using the following at command: AT^SCFG=”GPIO/mode/DAI”,”std” and this configuration is active after module’s restart.

Please note that level converters are required between the module‘s 1.8V digital audio lines and the 3.0V audio codec interface lines. Possible level converters are for example 74VHC1GT50 (up) and 74LVC1G34 (down) as shown in Figure 18 or mentioned in Section 2.3.1.

## 2.1.7.4 Electrical Characteristics of the Voiceband Part

### Setting Audio Parameters by AT Commands

The audio modes 2 to 10 can be temporarily adjusted according to the AT command parameter listed in the table below. The audio parameter is set with the AT command AT^SNFO and the audio mode is changed by AT^SNFS (see [1]). For a model of how the parameters influence the audio signal path see Section .

**Table 9:** Audio parameters adjustable by AT command

| Parameter | Influence to | Range | Gain range | Calculation |
|---|---|---|---|---|
| **AT^SNFI** | | | | |
| inVolStep | Digital TX volume | 0<br>1...100 | Mute<br>-43.5…+6dB | 0.5dB steps<br>(inVolStep-88)*0.5dB<br>88 = 0dB (default) |
| **AT^SNFO** | | | | |
| outVolStep | Digital RX volume | 0<br>1…100 | Mute<br>-43.5…+6dB | 0.5dB steps<br>(outVolStep-88)*0.5dB<br>88 = 0dB (default) |
| sideToneStep | Sidetone gain[1] | 0<br>0...175 | Mute<br>-43.5...<br>43.5dB | 0.5dB steps<br>SideToneStep*0.5dB<br>88 = 0dB |

1. The sidetone path contains two logically gain cells in series as shown in Figure 19. The first one can be controlled by the parameter sideToneGain while the second one will be controlled by outVolStep to keep the resulting sidetone gain constant independently of the RX Volume. The second cell introduces an offset of -37.5dB to the sidetone path. The resulting sidetone gain can be calculated according the following formula:
   Resulting sidetone gain = 0.5 * (sideToneStep - outVolStep) -37.5 [dB]

   If sideToneStep = 0 the sidetone path is completely muted - independent of outVolStep.

### Audio Programming Model

The audio programming model shows how the signal path can be influenced by varying AT command parameters: . For more information on the AT commands and parameters see Section and [1].

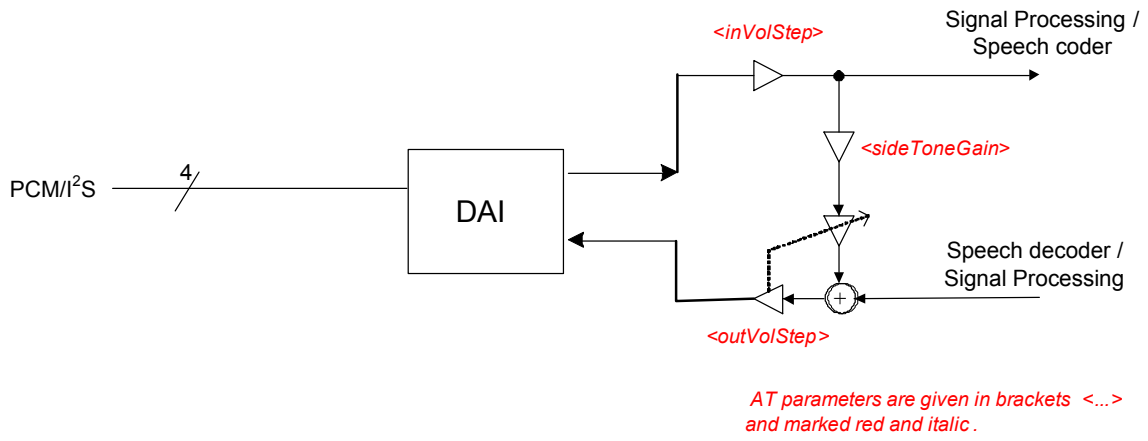



**Figure 19:** Audio programming model

**Characteristics of Audio Modes**
The electrical characteristics of the voiceband part depend on the current audio mode set with AT command. All values are noted for default gains, e.g. the default parameters are left unchanged.

Note: With regard to acoustic shock, the cellular application must be designed to avoid sending false AT commands that might increase amplification, e.g. for a highly sensitive earpiece. A protection circuit should be implemented in the cellular application.

## 2.1.8 RTC Backup

The internal Real Time Clock of ELS61-E R2 is supplied from a separate voltage regulator in the power supply component which is also active when ELS61-E R2 is in Power Down mode and BATT+ is available. An alarm function is provided that allows to wake up ELS61-E R2 without logging on to the RF network.

In addition, you can use the VDDLP pad to backup the RTC from an external capacitor. The capacitor is charged from the internal LDO of ELS61-E R2. If the voltage supply at BATT+ is disconnected the RTC can be powered by the capacitor. The size of the capacitor determines the duration of buffering when no voltage is applied to ELS61-E R2, i.e. the greater the capacitor the longer ELS61-E R2 will save the date and time. The RTC can also be supplied from an external battery (rechargeable or non-chargeable). In this case the electrical specification of the VDDLP pad (see Section 2.1.2) has to be taken in to account.

Figure 20 shows an RTC backup configuration. A serial 1kΩ resistor has to be placed on the application next to VDDLP. It limits the input current of an empty capacitor or battery.

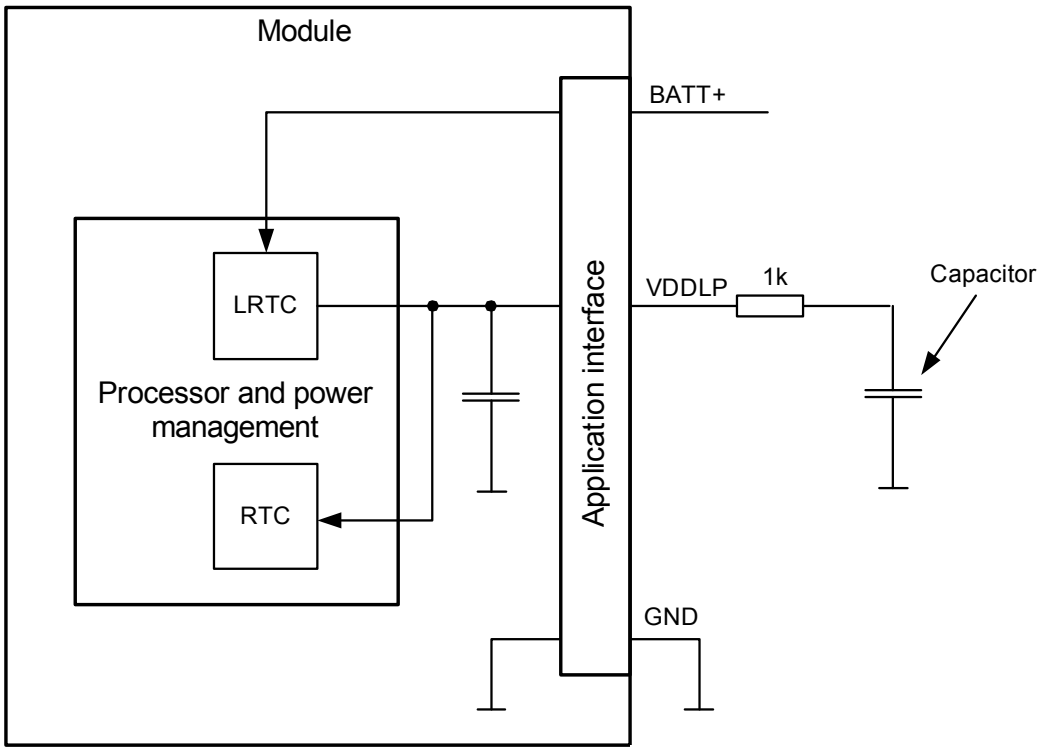



**Figure 20:** RTC supply variants

## 2.1.9 GPIO Interface

ELS61-E R2 offers a GPIO interface with 22 GPIO lines. The GPIO lines are shared with other interfaces or functions: Fast shutdown (see Section 2.1.14.4), status LED (see Section 2.1.14.1), the PWM functionality (see Section 2.1.12), an pulse counter (see Section 2.1.13), ASC0 (see Section 2.1.4), ASC1 (see Section 2.1.5), an SPI interface (see Section 2.1.11), and a DAI interface (see Section 2.1.7).

The following table shows the configuration variants for the GPIO pads. All variants are mutually exclusive, i.e. a pad configured for instance as Status LED is locked for alternative usage.

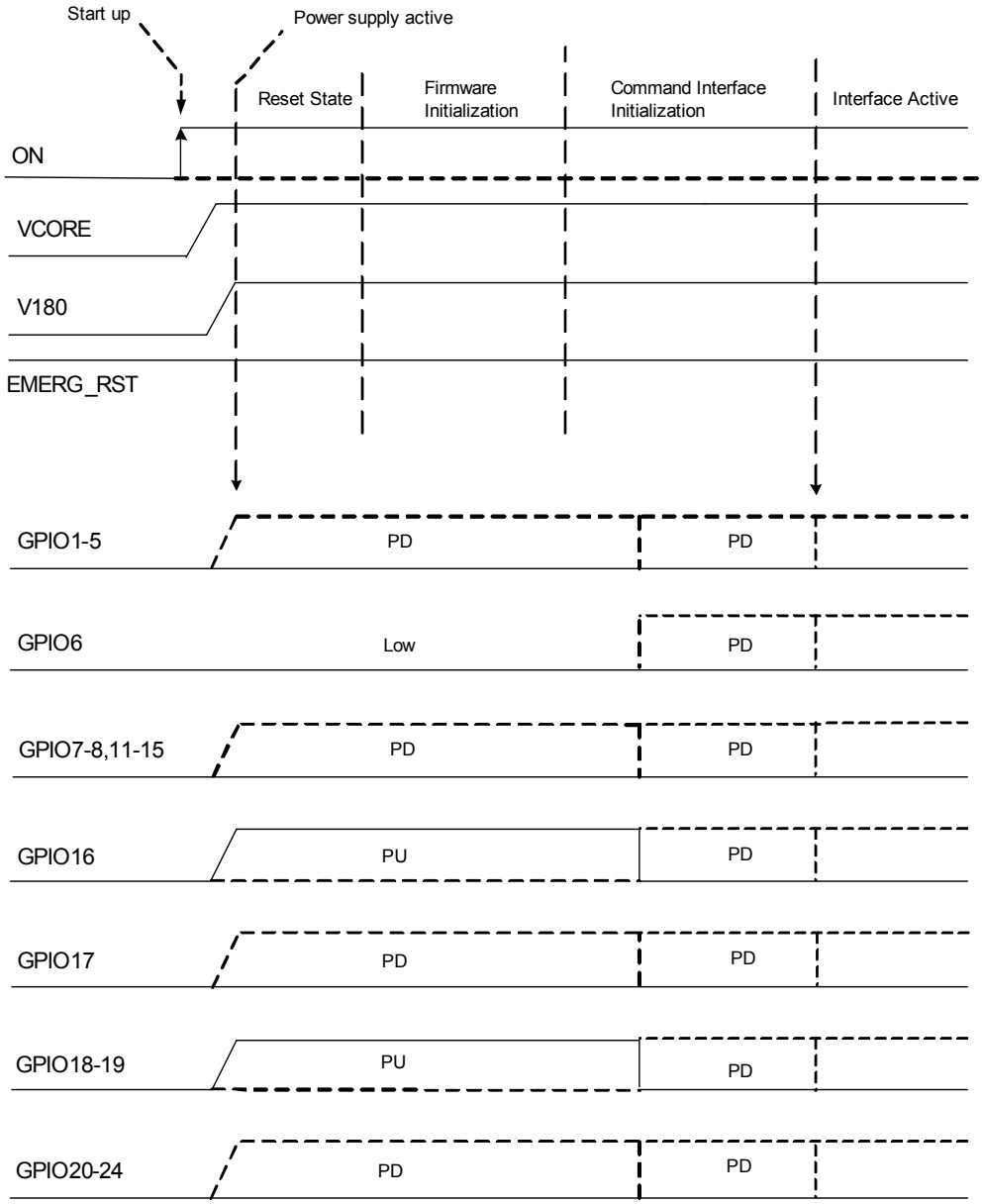
**Table 10:** GPIO lines and possible alternative assignment

| GPIO | Fast Shutdown | Status LED | PWM | Pulse Counter | ASC0 | ASC1 | SPI | DAI |
|---|---|---|---|---|---|---|---|---|
| GPIO1 | | | | | DTR0 | | | |
| GPIO2 | | | | | DCD0 | | | |
| GPIO3 | | | | | DSR0 | | SPI_CLK | |
| GPIO4 | FST_SHDN | | | | | | | MCLK[1] |
| GPIO5 | | Status LED | | | | | | |
| GPIO6 | | | PWM2 | | | | | |
| GPIO7 | | | PWM1 | | | | | |
| GPIO8 | | | | COUNTER | | | | |
| GPIO11 | | | | | | | | |
| GPIO12 | | | | | | | | |
| GPIO13 | | | | | | | | MCLK[1] |
| GPIO14 | | | | | | | | |
| GPIO15 | | | | | | | | |
| GPIO16 | | | | | | RXD1 | MOSI | |
| GPIO17 | | | | | | TXD1 | MISO | |
| GPIO18 | | | | | | RTS1 | | |
| GPIO19 | | | | | | CTS1 | SPI_CS | |
| GPIO20 | | | | | | | | DOUT |
| GPIO21 | | | | | | | | DIN |
| GPIO22 | | | | | | | | FSC |
| GPIO23 | | | | | | | | BCLK |
| GPIO24 | | | | | RING0 | | | |

1. The MCLK signal is optionally configurable for GPIO4 or GPIO13.

After startup, the above mentioned alternative GPIO line assignments can be configured using AT commands (see [1]). The configuration is non-volatile and available after module restart.

The following figure shows the startup behavior of the GPIO interface. With an active state of the ASC0 interface (i.e. CTS0 is at low level) the initialization of the GPIO interface lines is also finished.




*) For pull down values see Table 15.

**Figure 21:** GPIO startup behavior

## 2.1.10 I²C Interface

I²C is a serial, 8-bit oriented data transfer bus for bit rates up to 400kbps in Fast mode. It consists of two lines, the serial data line I2CDAT and the serial clock line I2CCLK. The module acts as a single master device, e.g. the clock I2CCLK is driven by the module. I2CDAT is a bi-directional line. Each device connected to the bus is software addressable by a unique 7-bit address, and simple master/slave relationships exist at all times. The module operates as master-transmitter or as master-receiver. The customer application transmits or receives data only on request of the module.

To configure and activate the I2C bus use the AT^SSPI command. Detailed information on the AT^SSPI command as well explanations on the protocol and syntax required for data transmission can be found in [1].

The I²C interface can be powered via the V180 line of ELS61-E R2. If connected to the V180 line, the I²C interface will properly shut down when the module enters the Power Down mode.

In the application I2CDAT and I2CCLK lines need to be connected to a positive supply voltage via a pull-up resistor. For electrical characteristics please refer to Table 2.

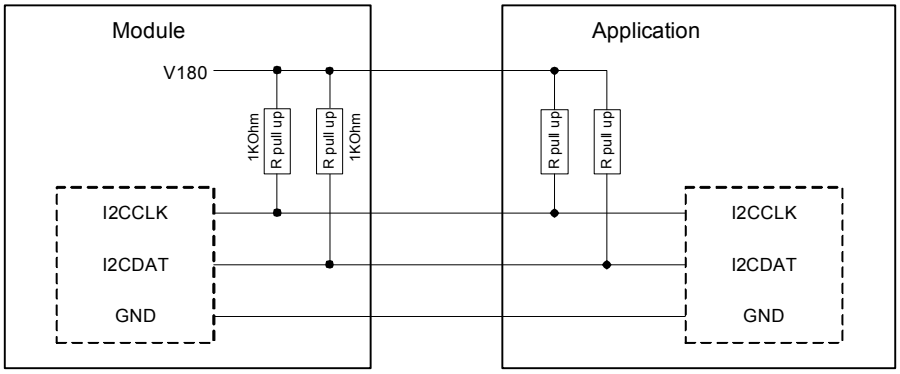



**Figure 22:** I²C interface connected to V180

Note: Good care should be taken when creating the PCB layout of the host application: The traces of I2CCLK and I2CDAT should be equal in length and as short as possible.

The following figure shows the startup behavior of the $I^2C$ interface. With an active state of the ASC0 interface (i.e. CTS0 is at low level) the initialization of the $I^2C$ interface is also finished.

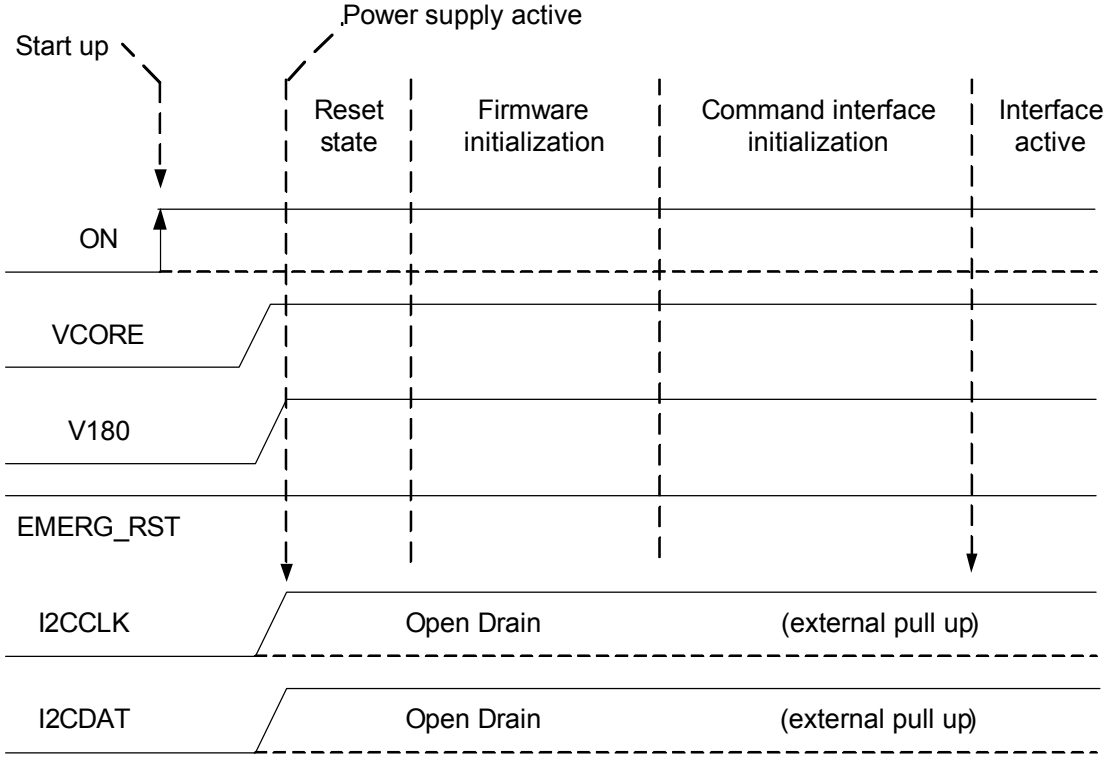



**Figure 23:** $I^2C$ startup behavior

### 2.1.11 SPI Interface

Four ELS61-E R2 GPIO interface lines can be configured as Serial Peripheral Interface (SPI). The SPI is a synchronous serial interface for control and data transfer between ELS61-E R2 and the external application. Only one application can be connected to the SPI and the interface supports only master mode. The transmission rates are up to 6.5Mbit/s. The SPI interface comprises the two data lines MOSI and MISO, the clock line SPI_CLK a well as the chip select line SPI_CS.

The four GPIO lines can be configured as SPI interface signals as follows: GPIO3 --> SPI_CLK, GPIO16 --> MOSI, GPIO17 --> MISO and GPIO19 --> SPI_CS. The configuration is done by AT command (see [1]). It is non-volatile and becomes active after a module restart.

The GPIO lines are also shared with the ASC1 signal lines and the ASC0 modem status signal line DSR0.

To configure and activate the SPI interface use the AT^SSPI command. Detailed information on the AT^SSPI command as well explanations on the SPI modes required for data transmission can be found in [1].

In general, SPI supports four operation modes. The modes are different in clock phase and clock polarity. The module's SPI mode can be configured by using the AT command AT^SSPI. Make sure the module and the connected slave device works with the same SPI mode.

Figure 24 shows the characteristics of the four SPI modes. The SPI modes 0 and 3 are the most common used modes. For electrical characteristics please refer to Table 2.

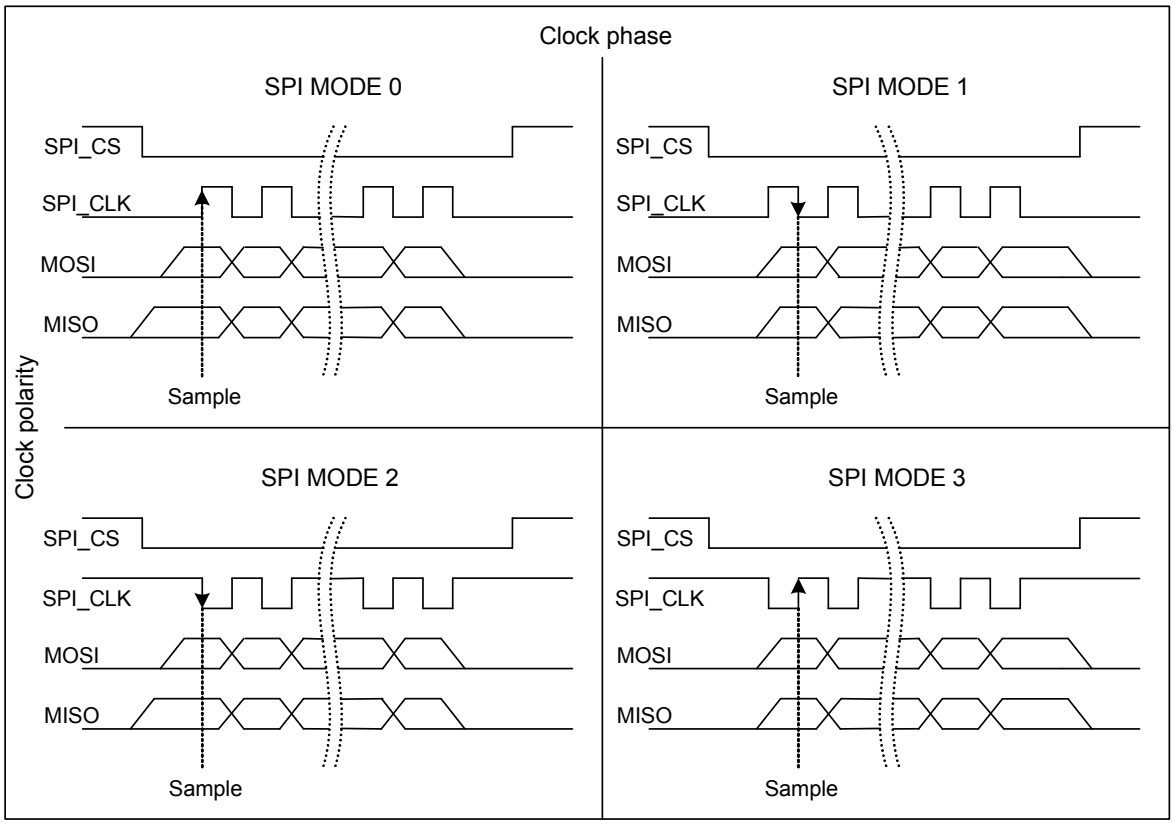



**Figure 24:** Characteristics of SPI modes

### 2.1.12 PWM Interfaces

The GPIO6 and GPIO7 interface lines can be configured as Pulse Width Modulation interface lines PWM1 and PWM2. The PWM interface lines can be used, for example, to connect buzzers. The PWM1 line is shared with GPIO7 and the PWM2 line is shared with GPIO6 (for GPIOs see Section 2.1.9). GPIO and PWM functionality are mutually exclusive.

The startup behavior of the lines is shown in Figure 21.

### 2.1.13 Pulse Counter

The GPIO8 line can be configured as pulse counter line COUNTER. The pulse counter interface can be used, for example, as a clock (for GPIOs see Section 2.1.9).

### 2.1.14 Control Signals

#### 2.1.14.1 Status LED

The GPIO5 interface line can be configured to drive a status LED that indicates different operating modes of the module (for GPIOs see Section 2.1.9). GPIO and LED functionality are mutually exclusive.

To take advantage of this function connect an LED to the GPIO5/LED line as shown in Figure 25.

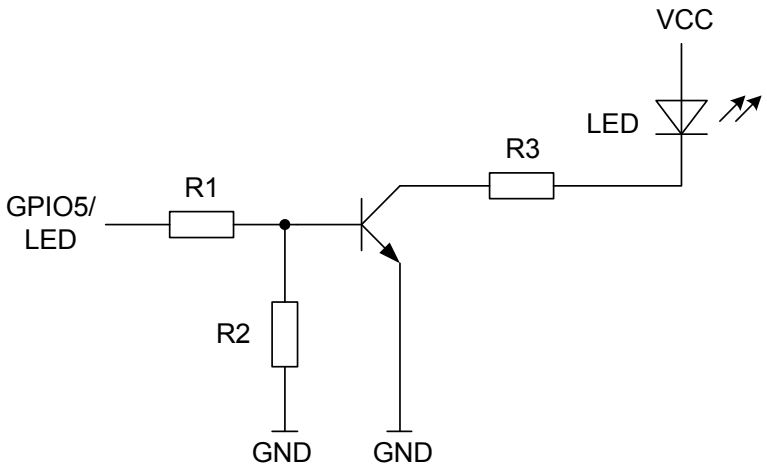



**Figure 25:** Status signaling with LED driver

### 2.1.14.2 Power Indication Circuit

In Power Down mode the maximum voltage at any digital or analog interface line must not exceed +0.3V (see also Section 2.1.2.1). Exceeding this limit for any length of time might cause permanent damage to the module.

It is therefore recommended to implement a power indication signal that reports the module's power state and shows whether it is active or in Power Down mode. While the module is in Power Down mode all signals with a high level from an external application need to be set to low state or high impedance state. The sample power indication circuit illustrated in Figure 26 denotes the module's active state with a low signal and the module's Power Down mode with a high signal or high impedance state.

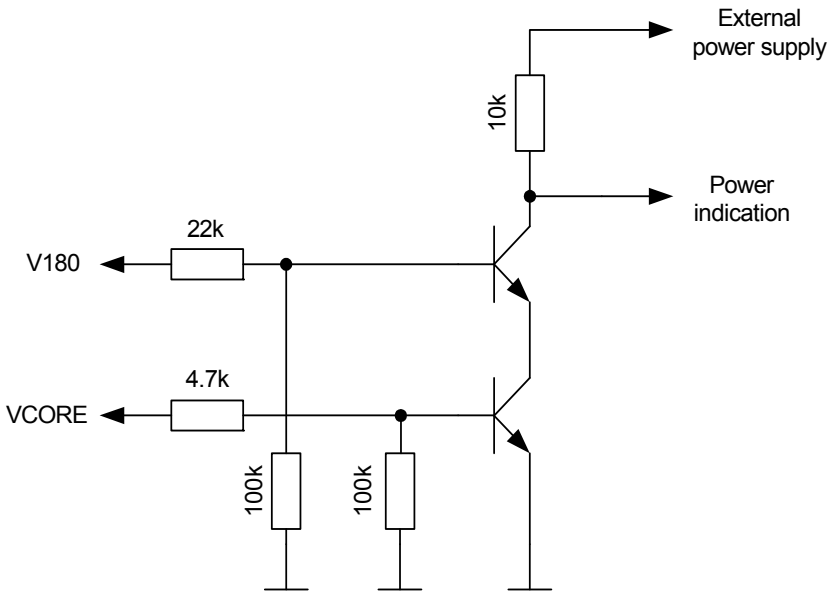



**Figure 26:** Power indication circuit

### 2.1.14.3 Host Wakeup

If no call, data or message transfer is in progress, the host may shut down its own USB interface to save power. If a call or other request (URC's, messages) arrives, the host can be notified of these events and be woken up again by a state transition of the ASC0 interface's RING0 line. This functionality should only be used with legacy USB applications not supporting the recommended USB suspend and resume mechanism as described in [6] (see also Section 2.1.3.1). For more information on how to configure the RING0 line by AT^SCFG command see [1].

Possible RING0 line states are listed in Table 11.

**Table 11:** Host wakeup lines

| Signal | I/O | Description |
|---|---|---|
| RING0 | O | Inactive to active low transition:<br>0 = The host shall wake up<br>1 = No wake up request |

### 2.1.14.4 Fast Shutdown

The GPIO4 interface line can be configured as fast shutdown signal line FST_SHDN. The configured FST_SHDN line is an active low control signal and must be applied for at least 1 milliseconds. If unused this line can be left open because of a configured internal pull-up resistor. Before setting the FST_SHDN line to low, the ON signal should be set to low (see Figure 27). Otherwise there might be back powering at the ON line in Power Down mode.

The fast shutdown feature can be triggered using the AT command AT^SMSO=<fso>. For details see [1].

If triggered, a low impulse >1 milliseconds on the FST_SHDN line starts the fast shutdown. The fast shutdown procedure still finishes any data activities on the module's flash file system, thus ensuring data integrity, but will no longer deregister gracefully from the network, thus saving the time required for network deregistration.

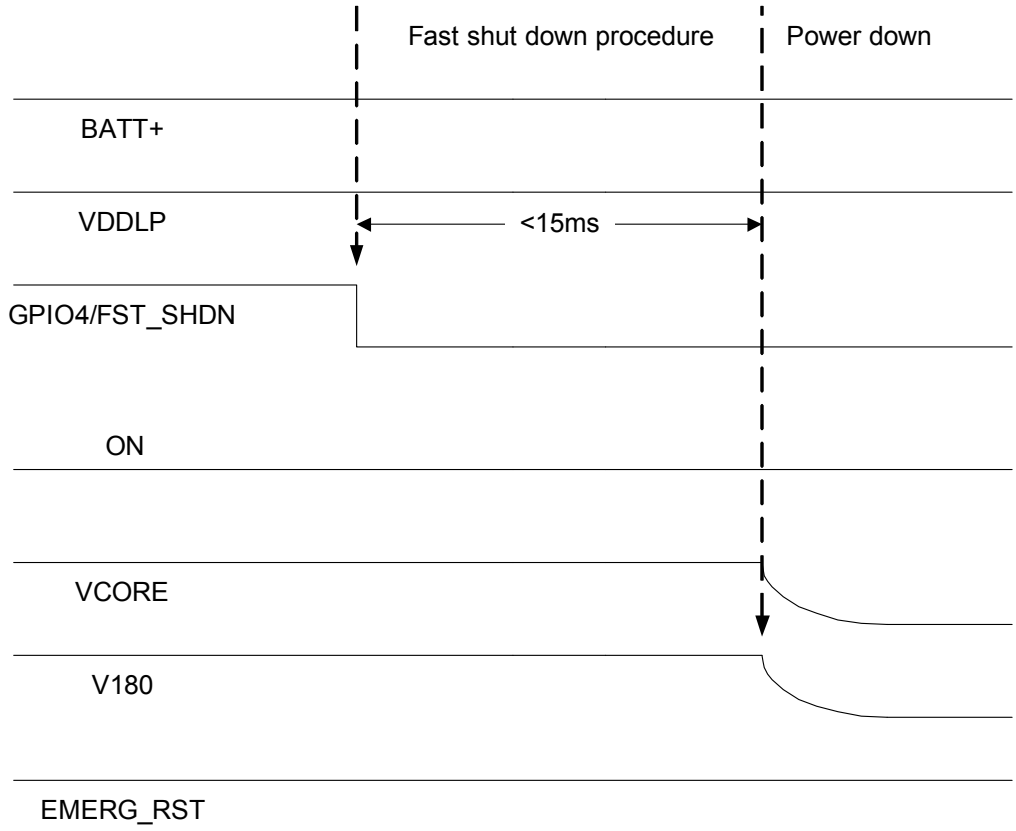



**Figure 27:** Fast shutdown timing

Please note that the normal software controlled shutdown using AT^SMSO will allow option for a fast shutdown by parameter <fso>, i.e., without network deregistration. However, in this case no URCs including shutdown URCs will be provided by the AT^SMSO command.

Please also note that the fast shutdown operation does not allow the module deregister from the network, therefore, this practice is not recommended, and should not be conducted on regular basis. If it is used for energy saving reason, for instance, used in battery-driven solutions that require prompt system shutdown before battery depletion, discretion is advised in such case.

## 2.2 RF Antenna Interface

The ELS61-E R2 GSM/UMTS/LTE antenna interface comprises a GSM/UMTS/LTE main antenna as well as a UMTS/LTE Rx diversity antenna to improve signal reliability and quality[1]. The RF interface has an impedance of 50Ω. ELS61-E R2 is capable of sustaining a total mismatch at the antenna line without any damage, even when transmitting at maximum RF power.

The external antenna must be matched properly to achieve best performance regarding radiated power, modulation accuracy and harmonic suppression. Antenna matching networks are not included on the ELS61-E R2 module and should be placed in the host application if the antenna does not have an impedance of 50Ω.

Regarding the return loss ELS61-E R2 provides the following values in the active band:

**Table 12:** Return loss in the active band

| State of module | Return loss of module | Recommended return loss of application |
|---|---|---|
| Receive | ≥ 8dB | ≥ 12dB |
| Transmit | not applicable | ≥ 12dB |

### 2.2.1 Antenna Interface Specifications

The LTE Cat.1 standard is designed for two antennas. It is mandatory to connect/apply the Rx diversity antenna to an existing antenna. The minimum efficiency shall be better than 50%.

**Table 13:** RF Antenna interface GSM/UMTS/LTE (at operating temperature range[1])

| Parameter | Conditions | Min. | Typical | Max. | Unit |
|---|---|---|---|---|---|
| LTE connectivity[2] | Band 1, 3, 8, 20, 28 | | | | |
| Receiver Input Sensitivity @ ARP (Dual Antenna; ch. bandwidth 5MHz) | LTE 700 Band 28 | -98.5 | -102.5 | | dBm |
| | LTE 800 Band 20 | -97 | -102 | | dBm |
| | LTE 900 Band 8 | -97 | -103 | | dBm |
| | LTE 1800 Band 3 | -97 | -102 | | dBm |
| | LTE 2100 Band 1 | -100 | -103 | | dBm |
| RF Power @ ARP with 50Ω Load (Board temperature < 85°C, BW:5MHz RB:25 (DL), 1 (UL) QPSK) | LTE 700 Band 28 | +21 | +23 | | dBm |
| | LTE 800 Band 20 | +21 | +23 | | dBm |
| | LTE 900 Band 8 | +21 | +23 | | dBm |
| | LTE 1800 Band 3 | +21 | +23 | | dBm |
| | LTE 2100 Band 1 | +21 | +23 | | dBm |

1. By delivery default the UMTS/LTE Rx diversity antenna is configured as available for the module since its usage is mandatory for LTE. Please refer to [1] for details on how to configure antenna settings.

**Table 13:** RF Antenna interface GSM/UMTS/LTE (at operating temperature range[1])

| Parameter | | Conditions | Min. | Typical | Max. | Unit |
|---|---|---|---|---|---|---|
| UMTS/HSPA connectivity[2] | | Band I, VIII | | | | |
| Receiver Input Sensitivity @ ARP | | UMTS 2100 Band I | -104.7 | -110 | | dBm |
| | | UMTS 900 Band VIII | -103.7 | -110 | | dBm |
| RF Power @ ARP with 50Ω Load (Board temperature < 85°C) | | UMTS 2100 Band I | +21 | +23.5 | | dBm |
| | | UMTS 900 Band VIII | +21 | +23.5 | | dBm |
| GPRS coding schemes | | Class 12, CS1 to CS4 | | | | |
| EGPRS | | Class 12, MCS1 to MCS9 | | | | |
| GSM Class | | Small MS | | | | |
| Static Receiver input Sensitivity @ ARP | | GSM 900 | -102 | -110 | | dBm |
| | | GSM 1800 | -102 | -109 | | dBm |
| RF Power @ ARP with 50Ω Load | GSM | GSM 900 | | 32.5 | | dBm |
| | | GSM 1800 | | 29.5 | | dBm |
| RF Power @ ARP with 50Ω Load, (**ROPR = 0**, i.e. no reduction) | GPRS, 1 TX | GSM 900 | | 32.5 | | dBm |
| | | GSM 1800 | | 29.5 | | dBm |
| | EDGE, 1 TX | GSM 900 | | 27 | | dBm |
| | | GSM 1800 | | 26 | | dBm |
| | GPRS, 2 TX | GSM 900 | | 32.5 | | dBm |
| | | GSM 1800 | | 29.5 | | dBm |
| | EDGE, 2 TX | GSM 900 | | 27 | | dBm |
| | | GSM 1800 | | 26 | | dBm |
| | GPRS, 3 TX | GSM 900 | | 32.5 | | dBm |
| | | GSM 1800 | | 29.5 | | dBm |
| | EDGE, 3 TX | GSM 900 | | 27 | | dBm |
| | | GSM 1800 | | 26 | | dBm |
| | GPRS, 4 TX | GSM 900 | | 32.5 | | dBm |
| | | GSM 1800 | | 29.5 | | dBm |
| | EDGE, 4 TX | GSM 900 | | 27 | | dBm |
| | | GSM 1800 | | 26 | | dBm |

**Table 13:** RF Antenna interface GSM/UMTS/LTE (at operating temperature range[1])

| Parameter | | Conditions | Min. | Typical | Max. | Unit |
|---|---|---|---|---|---|---|
| RF Power @ ARP with 50Ω Load, (**ROPR = 1**) | GPRS, 1 TX | GSM 900 | | 32.5 | | dBm |
| | | GSM 1800 | | 29.5 | | dBm |
| | EDGE, 1 TX | GSM 900 | | 27 | | dBm |
| | | GSM 1800 | | 26 | | dBm |
| | GPRS, 2 TX | GSM 900 | | 32.5 | | dBm |
| | | GSM 1800 | | 29.5 | | dBm |
| | EDGE, 2 TX | GSM 900 | | 27 | | dBm |
| | | GSM 1800 | | 26 | | dBm |
| | GPRS, 3 TX | GSM 900 | | 31.5 | | dBm |
| | | GSM 1800 | | 28.5 | | dBm |
| | EDGE, 3 TX | GSM 900 | | 27 | | dBm |
| | | GSM 1800 | | 26 | | dBm |
| | GPRS, 4 TX | GSM 900 | | 30.5 | | dBm |
| | | GSM 1800 | | 27.5 | | dBm |
| | EDGE, 4 TX | GSM 900 | | 27 | | dBm |
| | | GSM 1800 | | 26 | | dBm |
| RF Power @ ARP with 50Ω Load, (**ROPR = 2**) | GPRS, 1 TX | GSM 900 | | 32.5 | | dBm |
| | | GSM 1800 | | 29.5 | | dBm |
| | EDGE, 1 TX | GSM 900 | | 27 | | dBm |
| | | GSM 1800 | | 26 | | dBm |
| | GPRS, 2 TX | GSM 900 | | 30.5 | | dBm |
| | | GSM 1800 | | 27.5 | | dBm |
| | EDGE, 2 TX | GSM 900 | | 27 | | dBm |
| | | GSM 1800 | | 26 | | dBm |
| | GPRS, 3 TX | GSM 900 | | 29.5 | | dBm |
| | | GSM 1800 | | 26.5 | | dBm |
| | EDGE, 3 TX | GSM 900 | | 27 | | dBm |
| | | GSM 1800 | | 26 | | dBm |
| | GPRS, 4 TX | GSM 900 | | 28.5 | | dBm |
| | | GSM 1800 | | 25.5 | | dBm |
| | EDGE, 4 TX | GSM 900 | | 27 | | dBm |
| | | GSM 1800 | | 26 | | dBm |

**Table 13:** RF Antenna interface GSM/UMTS/LTE (at operating temperature range[1])

| Parameter | | Conditions | Min. | Typical | Max. | Unit |
|---|---|---|---|---|---|---|
| RF Power @ ARP with 50Ω Load, (**ROPR = 3**) | GPRS, 1 TX | GSM 900 | | 32.5 | | dBm |
| | | GSM 1800 | | 29.5 | | dBm |
| | EDGE, 1 TX | GSM 900 | | 27 | | dBm |
| | | GSM 1800 | | 26 | | dBm |
| | GPRS, 2 TX | GSM 900 | | 29.5 | | dBm |
| | | GSM 1800 | | 26.5 | | dBm |
| | EDGE, 2 TX | GSM 900 | | 27 | | dBm |
| | | GSM 1800 | | 26 | | dBm |
| | GPRS, 3 TX | GSM 900 | | 27.5 | | dBm |
| | | GSM 1800 | | 24.5 | | dBm |
| | EDGE, 3 TX | GSM 900 | | 27 | | dBm |
| | | GSM 1800 | | 26 | | dBm |
| | GPRS, 4 TX | GSM 900 | | 26.5 | | dBm |
| | | GSM 1800 | | 23.5 | | dBm |
| | EDGE, 4 TX | GSM 900 | | 27 | | dBm |
| | | GSM 1800 | | 26 | | dBm |
| RF Power @ ARP with 50Ω Load, (**ROPR = 4**, i.e. maximum reduction) | GPRS, 1 TX | GSM 900 | | 32.5 | | dBm |
| | | GSM 1800 | | 29.5 | | dBm |
| | EDGE, 1 TX | GSM 900 | | 27 | | dBm |
| | | GSM 1800 | | 26 | | dBm |
| | GPRS, 2 TX | GSM 900 | | 29.5 | | dBm |
| | | GSM 1800 | | 26.5 | | dBm |
| | EDGE, 2 TX | GSM 900 | | 24 | | dBm |
| | | GSM 1800 | | 23 | | dBm |
| | GPRS, 3 TX | GSM 900 | | 27.5 | | dBm |
| | | GSM 1800 | | 24.5 | | dBm |
| | EDGE, 3 TX | GSM 900 | | 22 | | dBm |
| | | GSM 1800 | | 21 | | dBm |
| | GPRS, 4 TX | GSM 900 | | 26.5 | | dBm |
| | | GSM 1800 | | 23.5 | | dBm |
| | EDGE, 4 TX | GSM 900 | | 21 | | dBm |
| | | GSM 1800 | | 20 | | dBm |

1. No active power reduction is implemented - any deviations are hardware related.
2. Applies also to UMTS/LTE Rx diversity antenna.

## 2.2.2 Antenna Installation

The antenna is connected by soldering the antenna pad (ANT_MAIN or ANT_DRX) and its neighboring ground pads (GND) directly to the application's PCB. The antenna pads are the antenna reference points (ARP) for ELS61-E R2. All RF data specified throughout this document is related to the ARP.

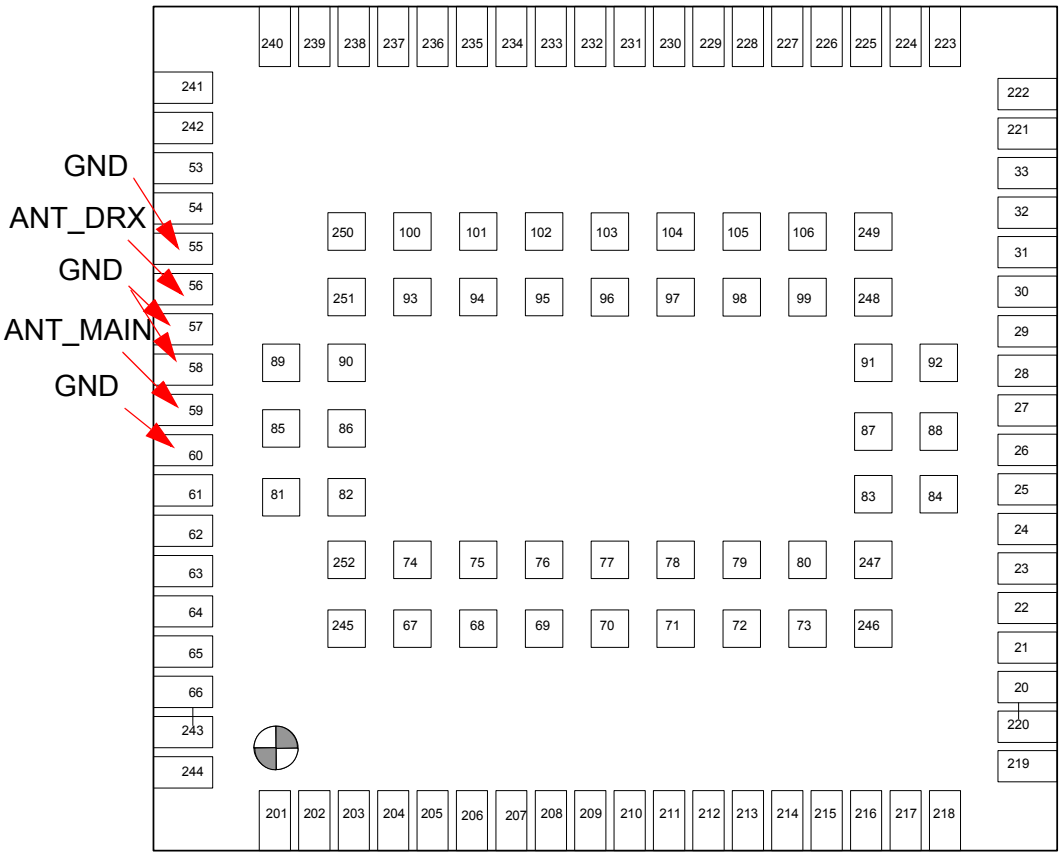



**Figure 28:** Antenna pads (bottom view)

The distance between the antenna pad and its neighboring GND pads has been optimized for best possible impedance. To prevent mismatch, special attention should be paid to these pads on the application's PCB.

The wiring of the antenna connection, starting from the antenna pad to the application's antenna should result in a 50Ω line impedance. Line width and distance to the GND plane needs to be optimized with regard to the PCB's layer stack. Some examples are given in Section 2.2.3.

To prevent receiver desensitization due to interferences generated by fast transients like high speed clocks on the external application PCB, it is recommended to realize the antenna connection line using embedded Stripline rather than Micro-Stripline technology. Please see Section 2.2.3.1 for examples of how to design the antenna connection in order to achieve the required 50Ω line impedance.

For type approval purposes, the use of a 50Ω coaxial antenna connector (U.FL-R-SMT) might be necessary. In this case the U.FL-R-SMT connector should be placed as close as possible to ELS61-E R2's antenna pad.

## 2.2.3 RF Line Routing Design

### 2.2.3.1 Line Arrangement Examples

Several dedicated tools are available to calculate line arrangements for specific applications and PCB materials - for example from http://www.polarinstruments.com/ (commercial software) or from http://web.awrcorp.com/Usa/Products/Optional-Products/TX-Line/ (free software).

**Embedded Stripline**
This figure below shows a line arrangement example for embedded stripline with 65µm FR4 prepreg (type: 1080) and 710µm FR4 core (4-layer PCB).

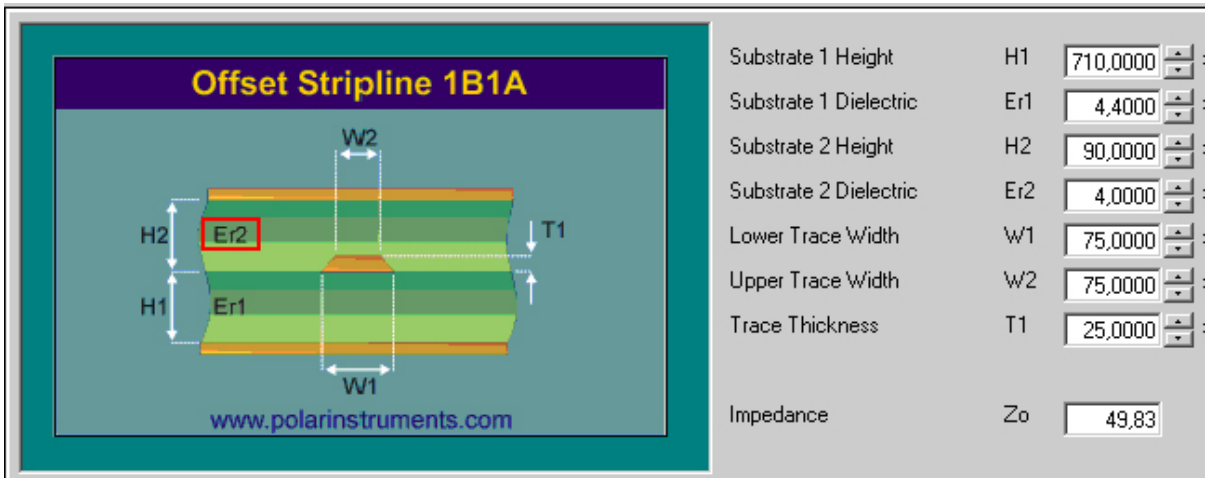



**Figure 29:** Embedded Stripline with 65µm prepreg (1080) and 710µm core

### Micro-Stripline

This section gives two line arrangement examples for micro-stripline.

- Micro-Stripline on 1.0mm Standard FR4 2-Layer PCB
  The following two figures show examples with different values for D1 (ground strip separation).

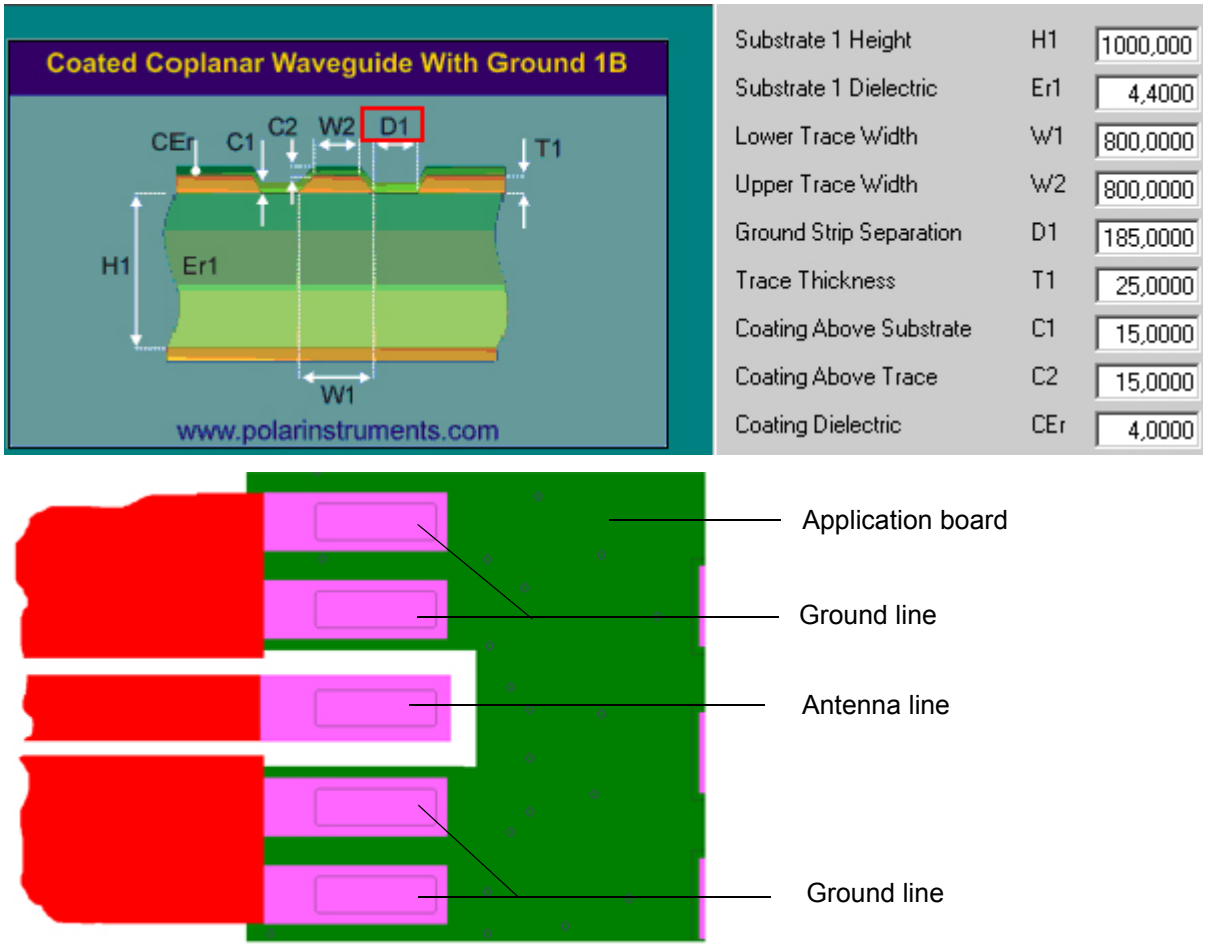



**Figure 30:** Micro-Stripline on 1.0mm standard FR4 2-layer PCB - example 1

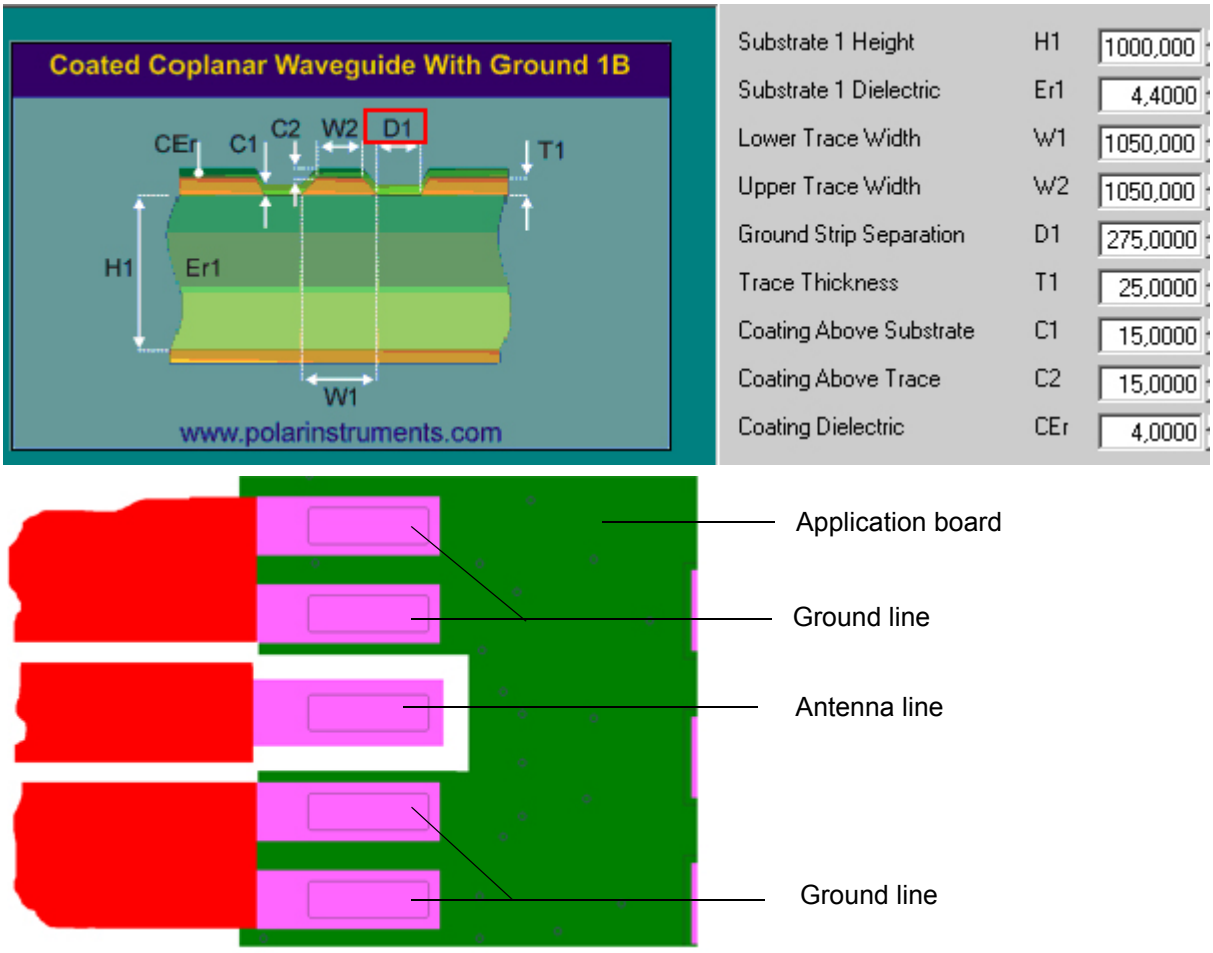



**Figure 31:** Micro-Stripline on 1.0mm Standard FR4 PCB - example 2

- Micro-Stripline on 1.5mm Standard FR4 2-Layer PCB
  The following two figures show examples with different values for D1 (ground strip separation).

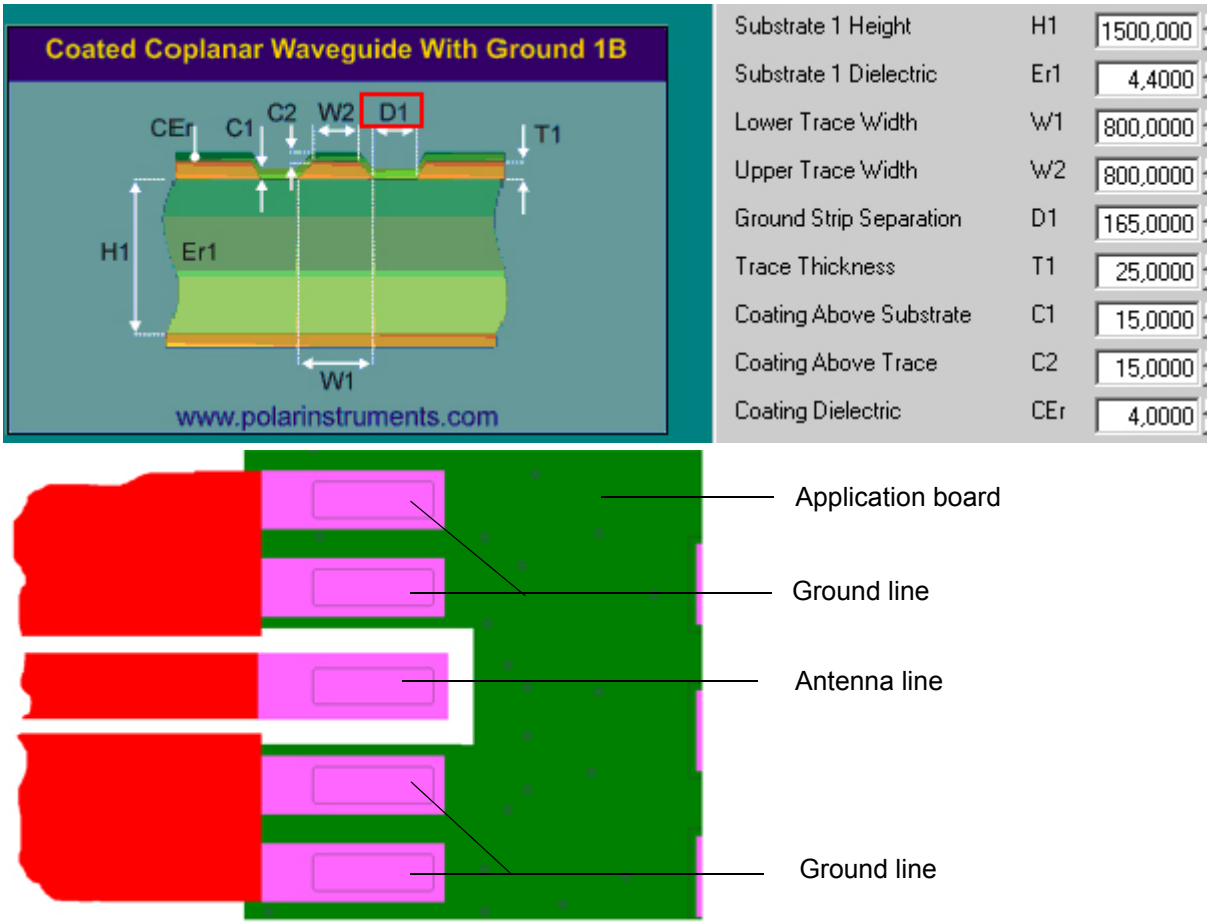



**Figure 32:** Micro-Stripline on 1.5mm Standard FR4 PCB - example 1

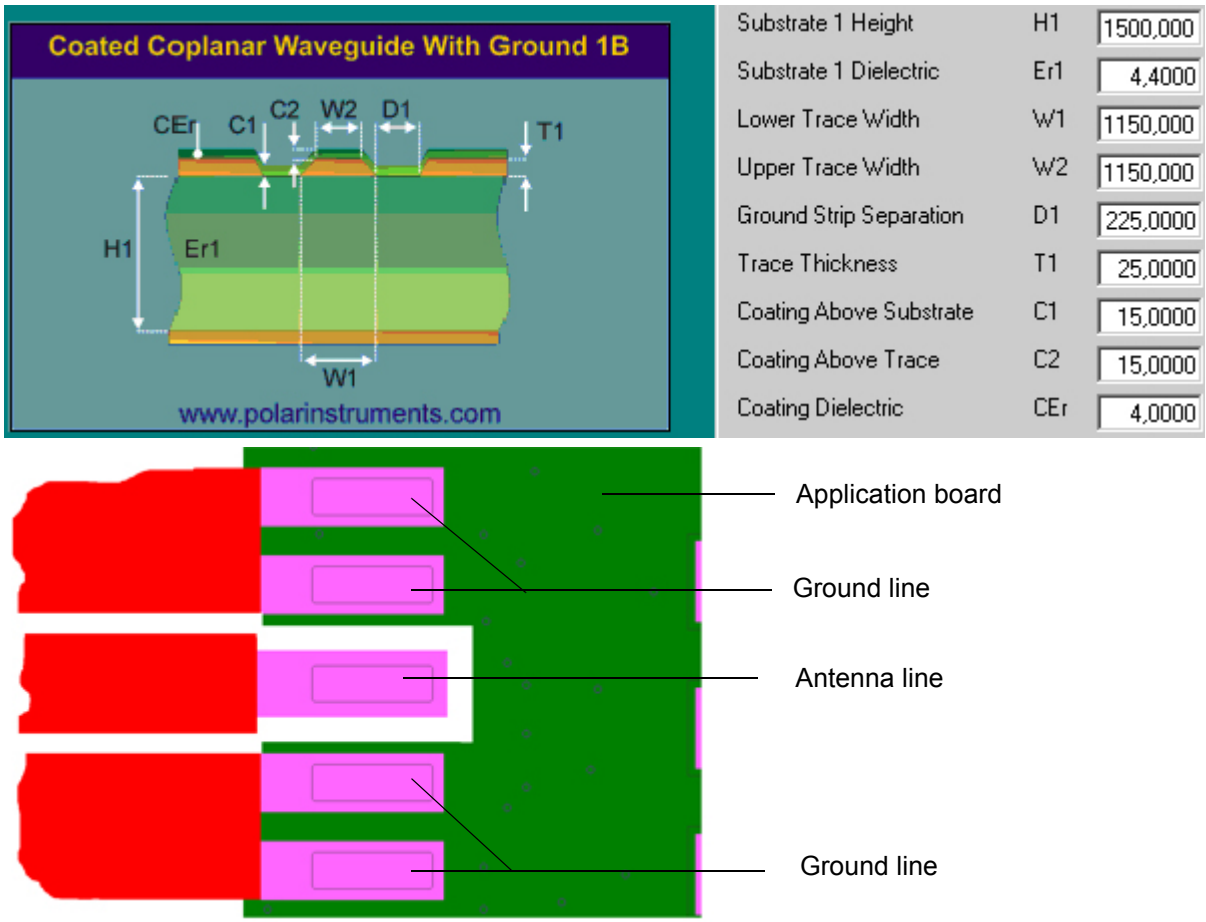



**Figure 33:** Micro-Stripline on 1.5mm Standard FR4 PCB - example 2

### 2.2.3.2 Routing Example

**Interface to RF Connector**

Figure 34 shows the connection of the module‘s antenna pad with an application PCB‘s coaxial antenna connector. Please note that the ELS61-E R2 bottom plane appears mirrored, since it is viewed from ELS61-E R2 top side. By definition the top of customer's board shall mate with the bottom of the ELS61-E R2 module.

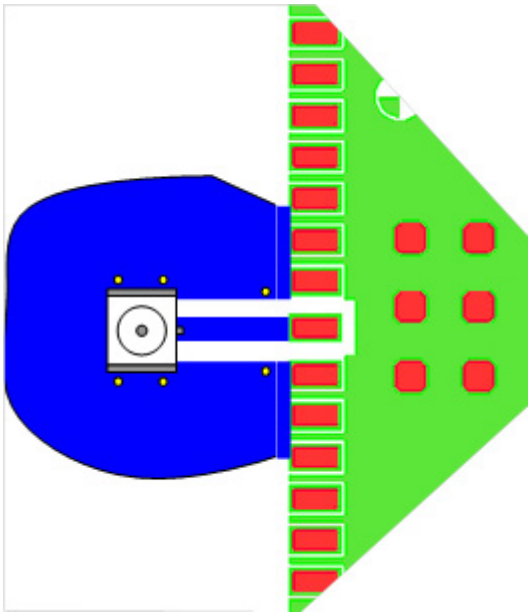


**Figure 34:** Routing to application‘s RF connector - top view

## 2.3 Sample Application

Figure 35 shows a typical example of how to integrate a ELS61-E R2 module with an application. Usage of the various host interfaces depends on the desired features of the application.

Because of the very low power consumption design, current flowing from any other source into the module circuit must be avoided, for example reverse current from high state external control lines. Therefore, the controlling application must be designed to prevent reverse current flow. Otherwise there is the risk of undefined states of the module during startup and shutdown or even of damaging the module.

Because of the high RF field density inside the module, it cannot be guaranteed that no self interference might occur, depending on frequency and the applications grounding concept. The potential interferers may be minimized by placing small capacitors (47pF) at suspected lines (e.g. RXD0, VDDLP, and ON).

**While developing SMT applications it is strongly recommended to provide test points for certain signals, i.e., lines to and from the module - for debug and/or test purposes. The SMT application should allow for an easy access to these signals. For details on how to implement test points see [4].**

The EMC measures are best practice recommendations. In fact, an adequate EMC strategy for an individual application is very much determined by the overall layout and, especially, the position of components.

Depending on the micro controller used by an external application ELS61-E R2's digital input and output lines may require level conversion. Section 2.3.1 shows a possible sample level conversion circuit.

Note: ELS61-E R2 is not intended for use with cables longer than 3m.

Disclaimer
No warranty, either stated or implied, is provided on the sample schematic diagram shown in Figure 35 and the information detailed in this section. As functionality and compliance with national regulations depend to a great amount on the used electronic components and the individual application layout manufacturers are required to ensure adequate design and operating safeguards for their products using ELS61-E R2 modules.

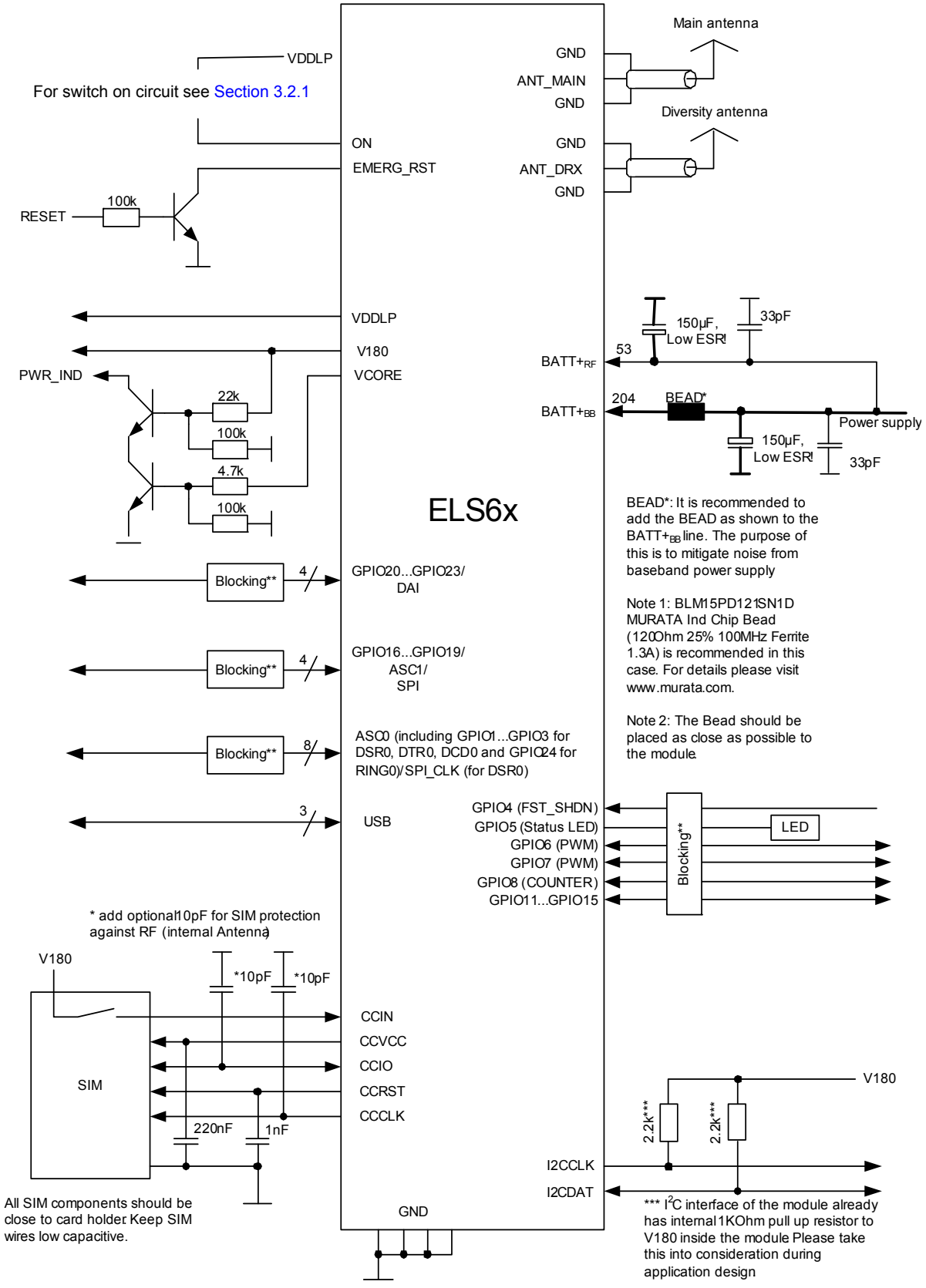



**Figure 35:** Schematic diagram of ELS61-E R2 sample application

### 2.3.1 Sample Level Conversion Circuit

Depending on the micro controller used by an external application ELS61-E R2's digital input and output lines (i.e., ASC0, ASC1 and GPIO lines) may require level conversion. The following Figure 36 shows a sample circuit with recommended level shifters for an external application's micro controller (with VLOGIC between 3.0V...3.6V). The level shifters can be used for digital input and output lines with $V_{OH}$max=1.85V or $V_{IH}$max =1.85V.

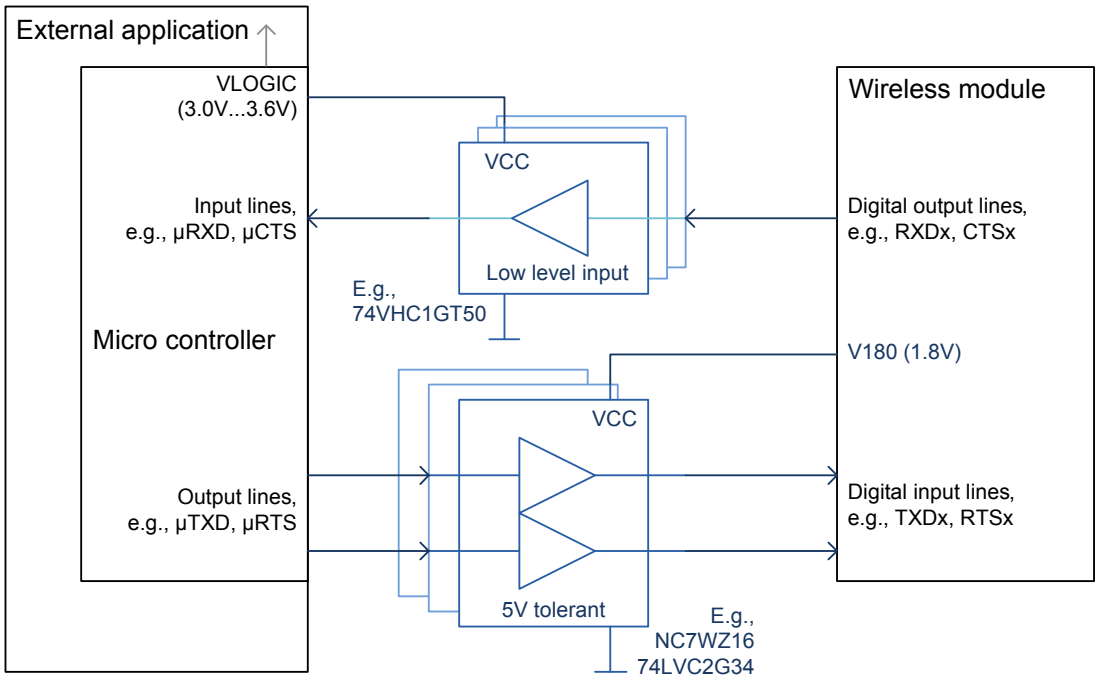



**Figure 36:** Sample level conversion circuit

# 3 Operating Characteristics

## 3.1 Operating Modes

The table below briefly summarizes the various operating modes referred to throughout the document.

**Table 14:** Overview of operating modes

| Mode | Function | |
|---|---|---|
| Normal operation | GSM / GPRS / UMTS / HSPA / LTE SLEEP | Power saving set automatically when no call is in progress and the USB connection is suspended by host or not present and no active communication via ASC0. |
| | GSM / GPRS / UMTS / HSPA / LTE IDLE | Power saving disabled or an USB connection not suspended, but no call in progress. |
| | GSM TALK/ GSM DATA | Connection between two subscribers is in progress. Power consumption depends on the GSM network coverage and several connection settings (e.g. DTX off/on, FR/EFR/HR, hopping sequences and antenna connection). The following applies when power is to be measured in TALK_GSM mode: DTX off, FR and no frequency hopping. |
| | GPRS DATA | GPRS data transfer in progress. Power consumption depends on network settings (e.g. power control level), uplink / downlink data rates and GPRS configuration (e.g. used multislot settings). |
| | EGPRS DATA | EGPRS data transfer in progress. Power consumption depends on network settings (e.g. power control level), uplink / downlink data rates and EGPRS configuration (e.g. used multislot settings). |
| | UMTS TALK/ UMTS DATA | UMTS data transfer in progress. Power consumption depends on network settings (e.g. TPC Pattern) and data transfer rate. |
| | HSPA DATA | HSPA data transfer in progress. Power consumption depends on network settings (e.g. TPC Pattern) and data transfer rate. |
| | LTE DATA | LTE data transfer in progress. Power consumption depends on network settings (e.g. TPC Pattern) and data transfer rate. |
| Power Down | Normal shutdown after sending the power down command. Only a voltage regulator is active for powering the RTC. Software is not active. Interfaces are not accessible. Operating voltage remains applied. | |
| Airplane mode | Airplane mode shuts down the radio part of the module, causes the module to log off from the network and disables all AT commands whose execution requires a radio connection. Airplane mode can be controlled by AT command (see [1]). | |
| Alarm mode | Restricted operation launched by RTC alert function when the module is in Power Down mode. In Alarm mode, the module remains deregistered from the network. Limited number of AT commands is accessible. | |

## 3.2 Power Up/Power Down Scenarios

In general, be sure not to turn on ELS61-E R2 while it is beyond the safety limits of voltage and temperature stated in Section 2.1.2.1. ELS61-E R2 immediately switches off after having started and detected these inappropriate conditions. In extreme cases this can cause permanent damage to the module.

### 3.2.1 Turn on ELS61-E R2

ELS61-E R2 can be turned on as described in the following sections:
- Connecting the operating voltage BATT+ (see Section 3.2.1.1).
- Hardware driven switch on by ON line: Starts Normal mode (see Section 3.2.1.2).

After startup or restart, the module will send the URC ^SYSSTART that notifies the host application that the first AT command can be sent to the module (see also [1]).

#### 3.2.1.1 Connecting ELS61-E R2 BATT+ Lines

Figure 37 shows sample external application circuits that allow to connect (and also to temporarily disconnect) the module‘s BATT+ lines from the external application‘s power supply.

Figure 37 illustrates the application of power employing an externally controlled microcontroller. The voltage supervisory circuit ensures that the power is disconnected and applied again depending on given thresholds.

The transistor T2 mentioned in Figure 37 should have an $R_{DS\_ON}$ value $\leq$ 50mΩ in order to minimize voltage drops.

Such circuits could be useful to maximize power savings for battery driven applications or to completely switch off and restart the module after a firmware update.

After connecting the BATT+ lines the module can then be (re-)started as described in Section 3.2.1.2 and Section 3.2.2.

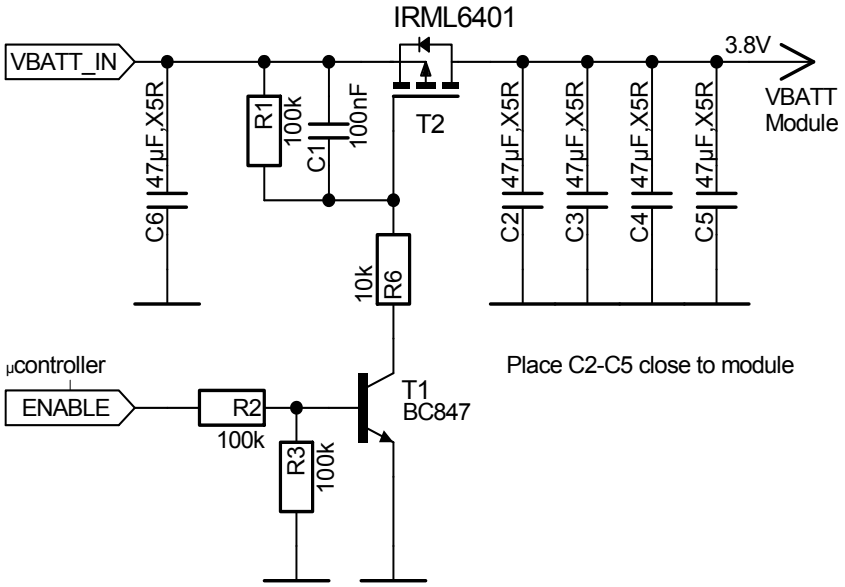



**Figure 37:** Sample circuit for applying power using an external µC

### 3.2.1.2 Switch on ELS61-E R2 Using ON Signal

After the operating voltage BATT+ is applied, ELS61-E R2 can be switched on by means of the ON signal.

The ON signal is an edge triggered signal and allows the input voltage level up to 5V. The module starts into normal mode on detecting the rising edge of the ON signal. The rising edge of ON signal must be applied at least 100 milliseconds later than BATT+. See Figure 39.

The following Figure 38 shows recommendations for possible switch-on circuits.

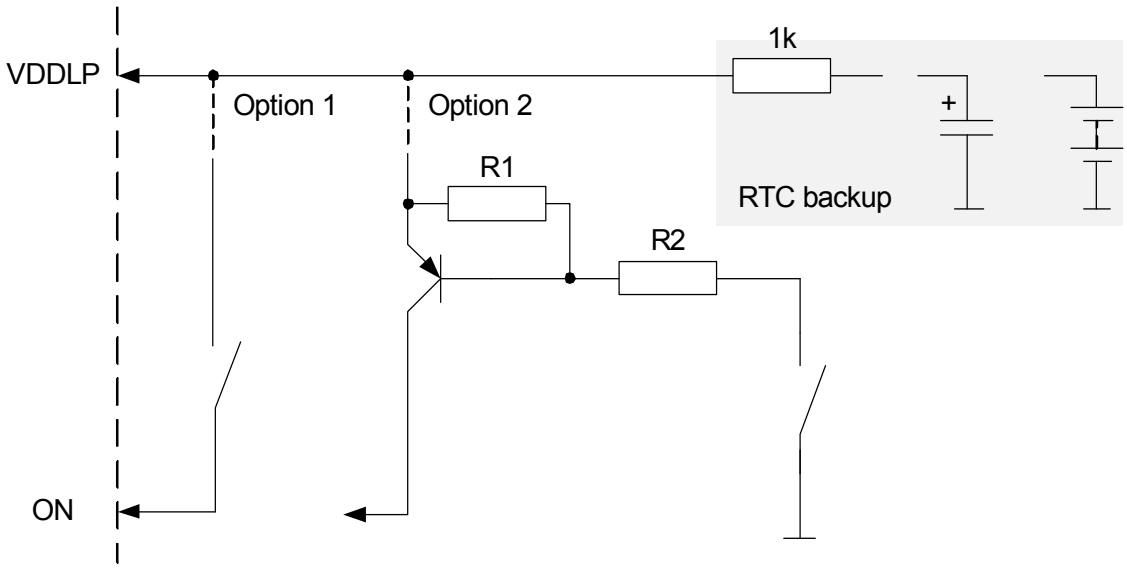



**Figure 38:** ON circuit options

It is recommended to set a serial 1kOhm resistor between the ON circuit and the external capacitor or battery at the VDDLP power supply (i.e., RTC backup circuit). This serial resistor protection is necessary in case the capacitor or battery has low power (is empty).With Option 2 the typical resistor values are: R1 = 150k and R2 = 3k. But the resistor values depend on the current gain from the employed PNP resistor.

Please note that the ON signal is an edge triggered signal. This implies that a micro-second high pulse on the signal line suffices to almost immediately switch on the module, as shown in Figure 39. After module startup the ON signal should always be set to low to prevent possible back powering at this pad.[1]

1. Please take due discretion when designing the filtering circuit, especially ESD, which may cause unintended switch on.

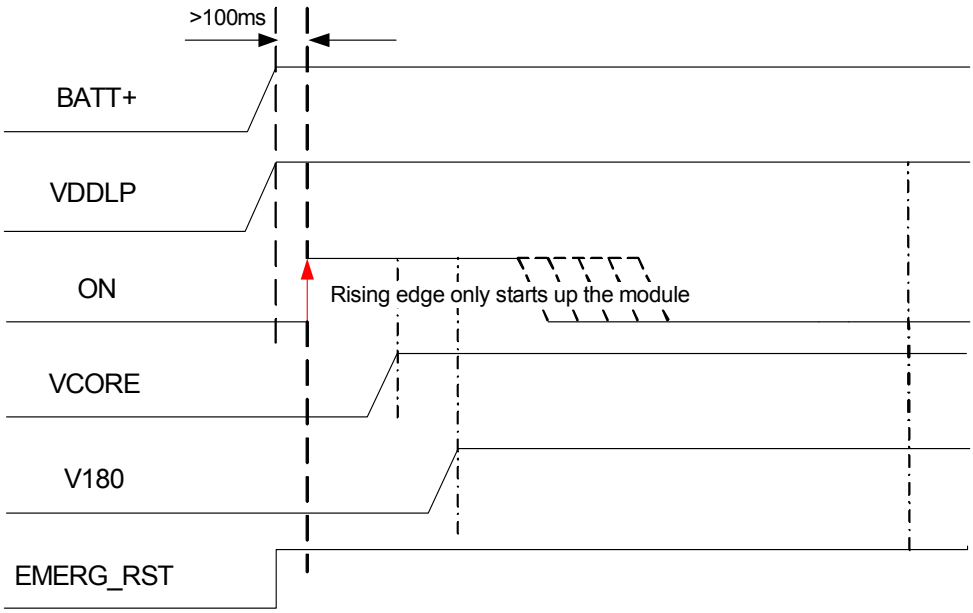



**Figure 39:** ON timing

### 3.2.1.3 Automatic Power On

In case an automatic power on function is required for an external module application, circuits such as shown in either Figure 40 or- if based on a voltage detector -Figure 42 and Figure 42 are recommended.

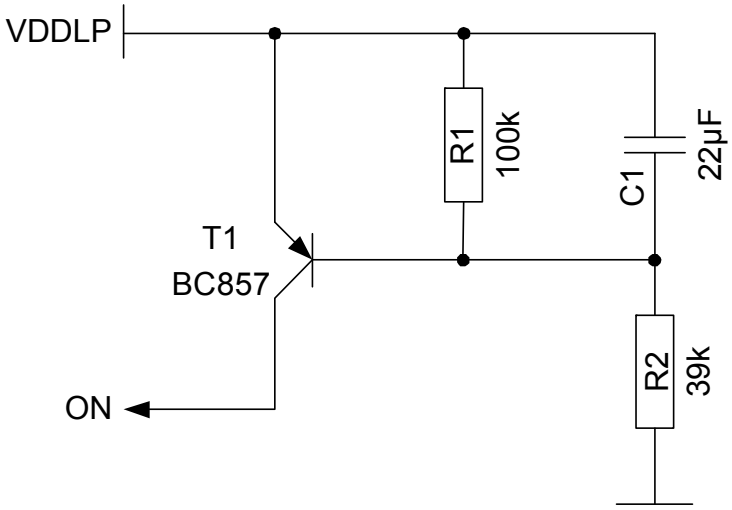



**Figure 40:** Automatic ON circuit

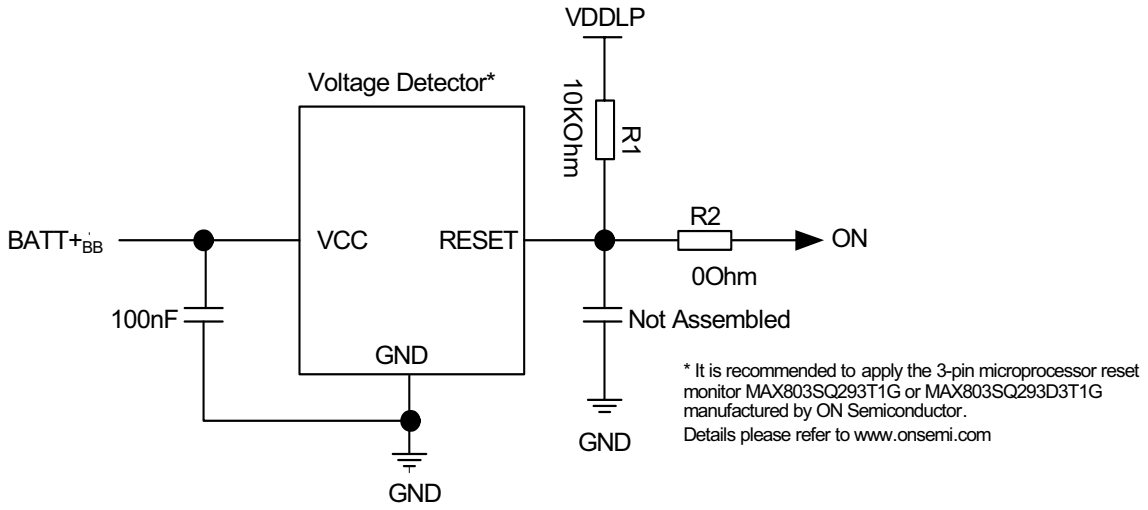



**Figure 41:** Automatic ON circuit based on voltage detector - option 1

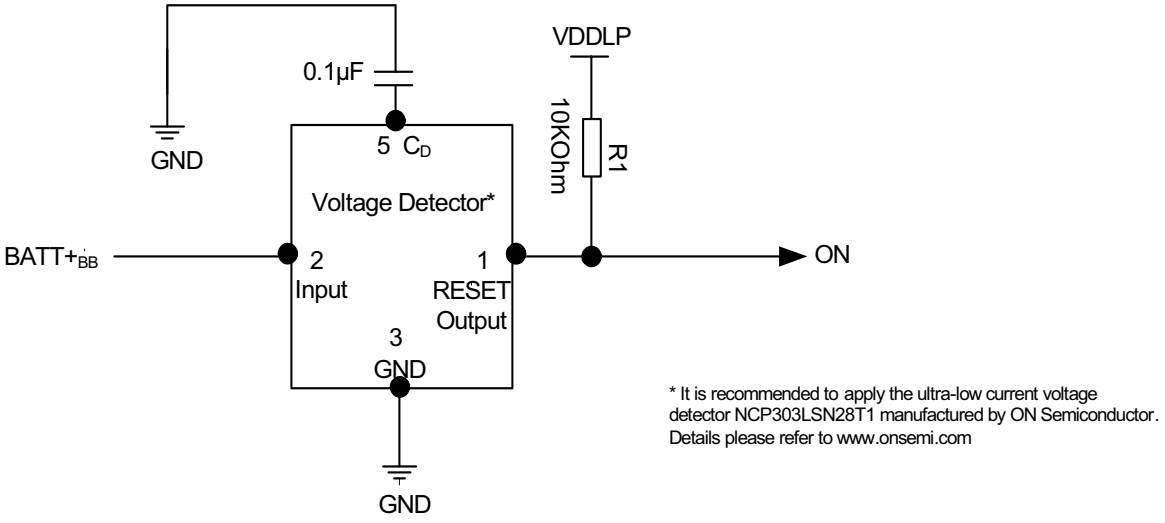



**Figure 42:** Automatic ON circuit based on voltage detector - option 2

## 3.2.2 Restart ELS61-E R2

After startup ELS61-E R2 can be re-started as described in the following sections:

- Software controlled reset by AT+CFUN command: Starts Normal mode (see Section 3.2.2.1).
- Hardware controlled reset by EMERG_RST line: Starts Normal mode (see Section 3.2.2.2).

### 3.2.2.1 Restart ELS61-E R2 via AT+CFUN Command

To reset and restart the ELS61-E R2 module use the command AT+CFUN. See [1] for details.

### 3.2.2.2 Restart ELS61-E R2 Using EMERG_RST

The EMERG_RST signal is internally connected to the main module processor. A low level for more than 10ms sets the processor and with it all the other signal pads to their respective reset state. The reset state is described in Section 3.2.3 as well as in the figures showing the startup behavior of an interface.

After releasing the EMERG-RST line, i.e., with a change of the signal level from low to high, the module restarts. The other signals continue from their reset state as if the module was switched on by the ON signal.

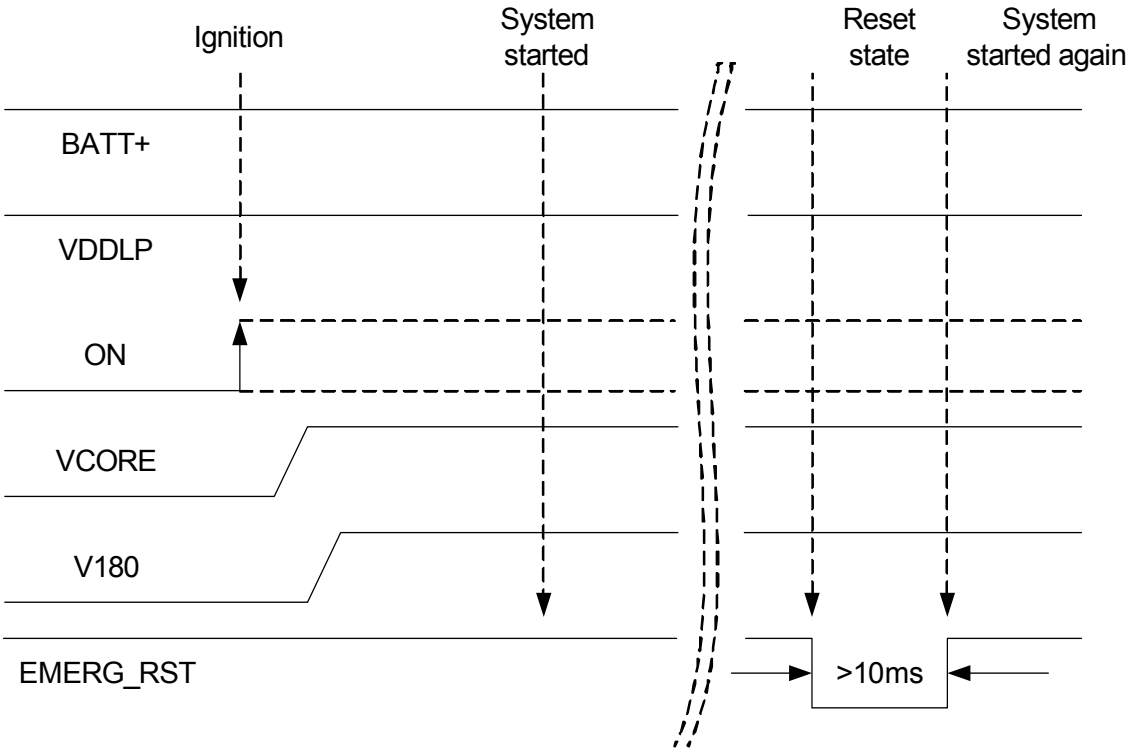



**Figure 43:** Emergency restart timing

It is recommended to control this EMERG_RST line with an open collector transistor or an open drain field-effect transistor.

*Caution: Use the EMERG_RST line only when, due to serious problems, the software is not responding for more than 5 seconds. Pulling the EMERG_RST line causes the loss of all information stored in the volatile memory. Therefore, this procedure is intended only for use in case of emergency, e.g. if ELS61-E R2 does not respond, if reset or shutdown via AT command fails.*

### 3.2.3 Signal States after Startup

Table 15 lists the states each interface signal passes through during reset phase and the first firmware initialization. For further firmware startup initializations the values may differ because of different GPIO line configurations.

The reset state is reached with the rising edge of the EMERG_RST signal - either after a normal module startup (see Section 3.2.1.2) or after a reset (see Section 3.2.2.2). After the reset state has been reached the firmware initialization state begins. The firmware initialization is completed as soon as the ASC0 interface lines CTS0, DSR0 and RING0 as well as the ASC1 interface line CTS1 have turned low (see Section 2.1.4 and Section 2.1.5). Now, the module is ready to receive and transmit data.

**Table 15:** Signal states

| Signal name | Reset state | First start up configuration |
|---|---|---|
| CCIO | L | O / L |
| CCRST | L | O / L |
| CCCLK | L | O / L |
| CCIN | T / 100k PD | I / PD |
| RXD0 | T / PU | O / H |
| TXD0 | T / PD | I |
| CTS0 | T / PU | O / H |
| RTS0 | T / PU | I / PD 110uA@1.8V |
| GPIO1 | T / PD | I / PD 110uA@1.8V |
| GPIO2 | T / PD | I / PD 30uA@1.8V |
| GPIO3 | T / PD | I / PD 110uA@1.8V |
| GPIO4 | T / PD | I / PD 110uA@1.8V |
| GPIO5 | T / PD | I / PD 30uA@1.8V |
| GPIO6 | L | I / PD 70uA@1.8V |
| GPIO7 | T / PD | I / PD 30uA@1.8V |
| GPIO8 | T / PD | I / PD 30uA@1.8V |
| GPIO11-GPIO13 | T / PD | I / PD 70uA@1.8V |
| GPIO14-GPIO15 | T / PU | I / PD 80uA@1.8V |
| GPIO16-GPIO20 | T / PD | I / PD 110uA@1.8V |
| GPIO21 | T / PD | I / PD 120uA@1.8V |
| GPIO22 | T / PD | I / PD 110uA@1.8V |
| GPIO23 | T / PD | I / PD 110uA@1.8V |
| GPIO24 | T / PD | I / PD 110uA@1.8V |
| I2CCLK | T / PU | T / PU |
| I2CDAT | T / PU | I / PU |

Note: The PD are On to always keep present even the GPIO is set to I (input).
Abbreviations used in above Table 15:

| | |
|---|---|
| L = Low level<br>H = High level<br>T = Tristate<br>I = Input | O = Output<br>OD = Open Drain<br>PD = Pull down<br>PU = Pull up |

### 3.2.4 Turn off ELS61-E R2

To switch the module off the following procedures may be used:
- *Software controlled shutdown procedure*: Software controlled by sending an AT command over the serial application interface. See Section 3.2.4.1.
- *Hardware controlled shutdown procedure*: Hardware controlled by disconnecting the module's power supply lines BATT+ (see Section 3.2.1.1).
- *Automatic shutdown (software controlled)*: See Section 3.2.5
  - Takes effect if ELS61-E R2 board temperature or voltage levels exceed a critical limit.

#### 3.2.4.1 Switch off ELS61-E R2 Using AT Command

The best and safest approach to powering down ELS61-E R2 is to issue the appropriate AT command. This procedure lets ELS61-E R2 log off from the network and allows the software to enter into a secure state and safe data before disconnecting the power supply. The mode is referred to as Power Down mode. In this mode, only the RTC stays active. After sending the switch off command AT^SMSO, be sure not to enter any further AT commands until the module was restarted.

CAUTION: Be sure not to disconnect the operating voltage $V_{BATT+}$ before V180 pad has gone low. Otherwise you run the risk of losing data, or in some rare cases even to render the module inoperable.

To monitor the V180 line, it is recommended to implement a power indication circuit as described in Section 2.1.14.2.

While ELS61-E R2 is in Power Down mode the application interface is switched off and must not be fed from any other voltage source. **Therefore, your application must be designed to avoid any current flow into any digital pads of the application interface.**

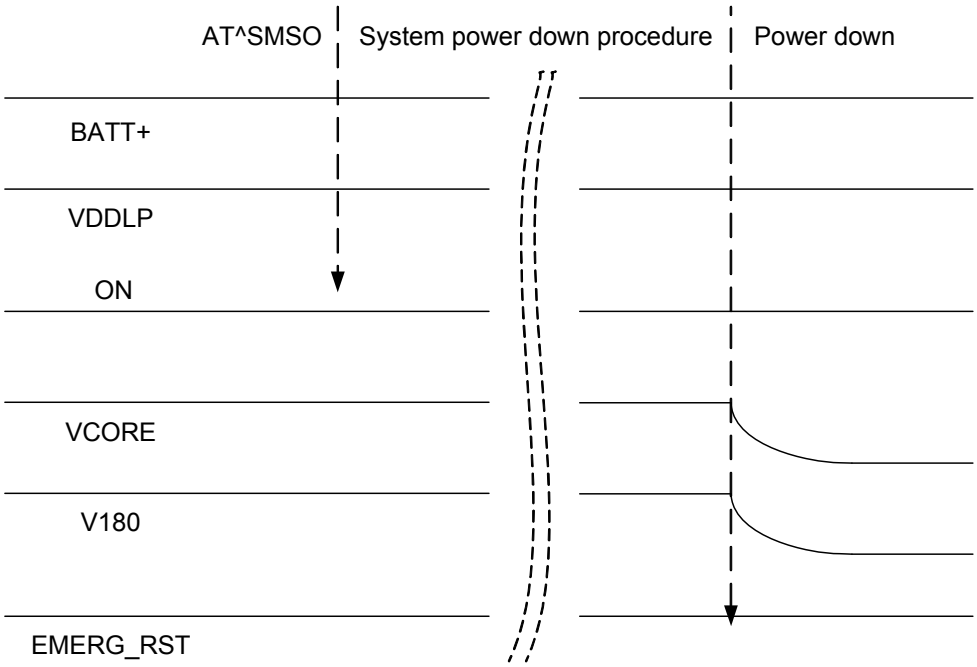



**Figure 44:** Switch off behavior

### 3.2.5 Automatic Shutdown

Automatic shutdown takes effect if the following event occurs:
- ELS61-E R2 board is exceeding the critical limits of overtemperature or undertemperature (see Section 3.2.5.1)
- Undervoltage or overvoltage is detected (see Section 3.2.5.2 and Section 3.2.5.3)

The automatic shutdown procedure is equivalent to the power-down initiated with an AT command, i.e. ELS61-E R2 logs off from the network and the software enters a secure state avoiding loss of data.

#### 3.2.5.1 Thermal Shutdown

The board temperature is constantly monitored by an internal NTC resistor located on the PCB. The values detected by the NTC resistor are measured directly on the board and therefore, are not fully identical with the ambient temperature.

Each time the board temperature goes out of range or back to normal, ELS61-E R2 instantly displays an alert (if enabled).
- URCs indicating the level "1" or "-1" allow the user to take appropriate precautions, such as protecting the module from exposure to extreme conditions. The presentation of the URCs depends on the settings selected with the AT^SCTM write command (for details see [1]):
  AT^SCTM=1: Presentation of URCs is always enabled.
  AT^SCTM=0 (default): Presentation of URCs is enabled during the 2 minute guard period after start-up of ELS61-E R2. After expiry of the 2 minute guard period, the presentation of URCs will be disabled, i.e. no URCs with alert levels "1" or "-1" will be generated.
- URCs indicating the level "2" or "-2" are instantly followed by an orderly shutdown. The presentation of these URCs is always enabled, i.e. they will be output even though the factory setting AT^SCTM=0 was never changed.

The maximum temperature ratings are stated in Section 3.6. Refer to Table 16 for the associated URCs.

**Table 16:** Temperature dependent behavior

| | |
|---|---|
| Sending temperature alert (2min after ELS61-E R2 start-up, otherwise only if URC presentation enabled) | |
| ^SCTM_B: 1 | Board close to overtemperature limit. |
| ^SCTM_B: -1 | Board close to undertemperature limit. |
| ^SCTM_B: 0 | Board back to non-critical temperature range. |
| Automatic shutdown (URC appears no matter whether or not presentation was enabled) | |
| ^SCTM_B: 2 | Alert: Board equal or beyond overtemperature limit. ELS61-E R2 switches off. |
| ^SCTM_B: -2 | Alert: Board equal or below undertemperature limit. ELS61-E R2 switches off. |

### 3.2.5.2 Undervoltage Shutdown

The undervoltage shutdown threshold is the specified minimum supply voltage $V_{BATT+}$ given in Table 2. When the average supply voltage measured by ELS61-E R2 approaches the undervoltage shutdown threshold (i.e., 0.05V offset) the module will send the following URC:

^SBC: Undervoltage Warning

The undervoltage warning is sent only once - until the next time the module is close to the undervoltage shutdown threshold.

If the voltage continues to drop below the specified undervoltage shutdown threshold, the module will send the following URC:

^SBC: Undervoltage Shutdown

This alert is sent only once before the module shuts down cleanly without sending any further messages.

This type of URC does not need to be activated by the user. It will be output automatically when fault conditions occur.

Note: For battery powered applications it is strongly recommended to implement a BATT+ connecting circuit as described in Section 3.2.1.1 in order to not only be able save power, but also to restart the module after an undervoltage shutdown where the battery is deeply discharged. Also note that the undervoltage threshold is calculated for max. 400mV voltage drops during transmit burst. Power supply sources for external applications should be designed to tolerate 400mV voltage drops without crossing the lower limit of 3.0 V. For external applications operating at the limit of the allowed tolerance the default undervoltage threshold may be adapted by subtracting an offset. For details see [1]: AT^SCFG= "MEShutdown/sVsup/threshold".

### 3.2.5.3 Overvoltage Shutdown

The overvoltage shutdown threshold is the specified maximum supply voltage $V_{BATT+}$ given in Table 2. When the average supply voltage measured by ELS61-E R2 approaches the overvoltage shutdown threshold (i.e., 0.05V offset) the module will send the following URC:

^SBC: Overvoltage Warning

The overvoltage warning is sent only once - until the next time the module is close to the overvoltage shutdown threshold.

If the voltage continues to rise above the specified overvoltage shutdown threshold, the module will send the following URC:

^SBC: Overvoltage Shutdown

This alert is sent only once before the module shuts down cleanly without sending any further messages.

This type of URC does not need to be activated by the user. It will be output automatically when fault conditions occur.

Keep in mind that several ELS61-E R2 components are directly linked to BATT+ and, therefore, the supply voltage remains applied at major parts of ELS61-E R2. Especially the power amplifier linked to $BATT+_{RF}$ is very sensitive to high voltage and might even be destroyed.

## 3.3 Automatic GPRS Multislot Class Change

Temperature control is also effective for operation in GPRS Multislot Class 10 or 12. If the board temperature increases to 75°C while data is transmitted over GPRS, the module automatically reverts from GPRS Multislot Class 12 (4Tx) or Class 10 (2Tx) to Class 8 (1Tx). This reduces the power consumption and, consequently, causes the board's temperature to decrease. Once the temperature drops to a 70°C, ELS61-E R2 returns to the higher Multislot Class. If the temperature stays at the critical level or even continues to rise, ELS61-E R2 will not switch back to the higher class.

After a transition from Multislot Class 12 or 10 to Multislot 8 a possible switchback to Multislot Class 12 or 10 is blocked for one minute.

Please note that there is not one single cause of switching over to a lower GPRS Multislot Class. Rather it is the result of an interaction of several factors, such as the board temperature that depends largely on the ambient temperature, the operating mode and the transmit power. Furthermore, take into account that there is a delay until the network proceeds to a lower or, accordingly, higher Multislot Class. The delay time is network dependent. In extreme cases, if it takes too much time for the network and the temperature cannot drop due to this delay, the module may even switch off as described in Section 3.2.5.1.

## 3.4 Power Saving

ELS61-E R2 can be configured in two ways to control power consumption:

- Using the AT command AT^SPOW it is possible to specify a so-called power saving mode for the module (<mode> = 2; for details on the command see [1]). The module's UART interfaces (ASC0 and ASC1) are then deactivated and will only periodically be activated to be able to listen to network paging messages as described in Section 3.4.1, Section 3.4.2 and Section 3.4.3. See Section 3.4.4 for a description on how to immediately wake up ELS61-E R2 again using RTS0.

  Please note that the AT^SPOW setting has no effect on the USB interface. As long as the USB connection is active, the module will not change into its SLEEP state to reduce its functionality to a minimum and thus minimizing its current consumption. To enable switching into SLEEP mode, the USB connection must therefore either not be present at all or the USB host must bring its USB interface into Suspend state. Also, VUSB_IN should always be kept enabled for this functionality. See "Universal Serial Bus Specification Revision 2.0"[1] for a description of the Suspend state.

- Using the AT command AT^SCFG="Radio/OutputPowerReduction" it is possible for the module in GPRS and EGPRS multislot scenarios to reduce its output power according to 3GPP 45.005 section. By default a maximum power reduction is enabled. For details on the command see [1].

### 3.4.1 Power Saving while Attached to GSM Networks

The power saving possibilities while attached to a GSM network depend on the paging timing cycle of the base station. The duration of a power saving interval can be calculated using the following formula:

t = 4.615 ms (TDMA frame duration) * 51 (number of frames) * DRX value.

DRX (Discontinuous Reception) is a value from 2 to 9, resulting in paging intervals between 0.47 and 2.12 seconds. The DRX value of the base station is assigned by the GSM network operator.

In the pauses between listening to paging messages, the module resumes power saving, as shown in Figure 45.

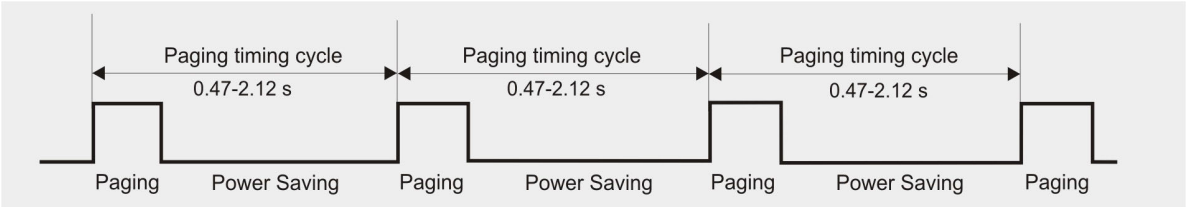



**Figure 45:** Power saving and paging in GSM networks

1. The specification is ready for download on http://www.usb.org/developers/docs/

The varying pauses explain the different potential for power saving. The longer the pause the less power is consumed.

Generally, power saving depends on the module's application scenario and may differ from the above mentioned normal operation. The power saving interval may be shorter than 0.47 seconds or longer than 2.12 seconds.

### 3.4.2 Power Saving while Attached to WCDMA Networks

The power saving possibilities while attached to a WCDMA network depend on the paging timing cycle of the base station.

During normal WCDMA operation, i.e., the module is connected to a WCDMA network, the duration of a power saving period varies. It may be calculated using the following formula:

$t = 2^{DRX\ value} * 10$ ms (WCDMA frame duration).

DRX (Discontinuous Reception) in WCDMA networks is a value between 6 and 9, thus resulting in power saving intervals between 0.64 and 5.12 seconds. The DRX value of the base station is assigned by the WCDMA network operator.

In the pauses between listening to paging messages, the module resumes power saving, as shown in Figure 46.

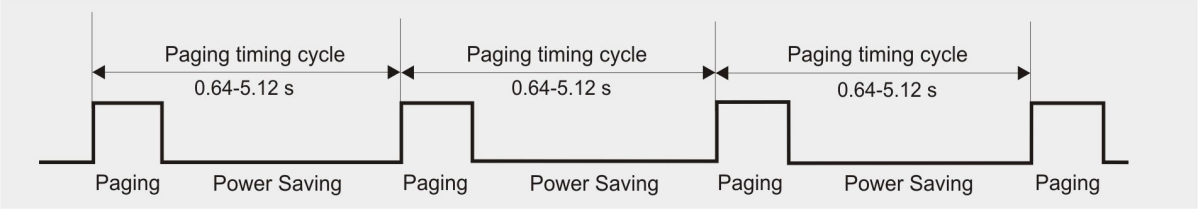



**Figure 46:** Power saving and paging in WCDMA networks

The varying pauses explain the different potential for power saving. The longer the pause the less power is consumed.

Generally, power saving depends on the module's application scenario and may differ from the above mentioned normal operation. The power saving interval may be shorter than 0.64 seconds or longer than 5.12 seconds.

### 3.4.3 Power Saving while Attached to LTE Networks

The power saving possibilities while attached to an LTE network depend on the paging timing cycle of the base station.

During normal LTE operation, i.e., the module is connected to an LTE network, the duration of a power saving period varies. It may be calculated using the following formula:

t = DRX Cycle Value * 10 ms

DRX cycle value in LTE networks is any of the four values: 32, 64, 128 and 256, thus resulting in power saving intervals between 0.32 and 2.56 seconds. The DRX cycle value of the base station is assigned by the LTE network operator.

In the pauses between listening to paging messages, the module resumes power saving, as shown in Figure 47.

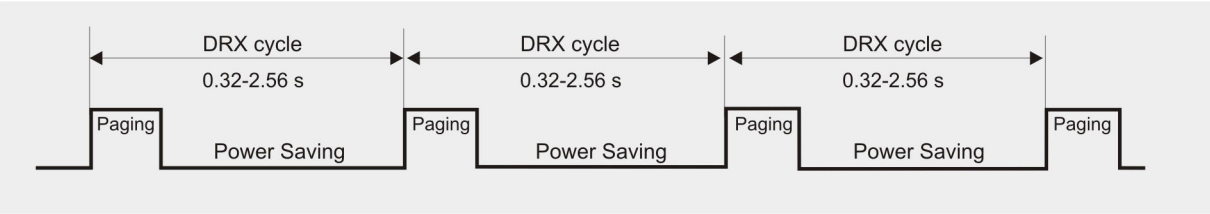



**Figure 47:** Power saving and paging in LTE networks

The varying pauses explain the different potential for power saving. The longer the pause the less power is consumed.

Generally, power saving depends on the module's application scenario and may differ from the above mentioned normal operation. The power saving interval may be shorter than 0.32 seconds or longer than 2.56 seconds.

### 3.4.4 Wake-up via RTS0

RTS0 can be used to wake up ELS61-E R2 from SLEEP mode configured with AT^SPOW. Assertion of RTS0 (i.e., toggle from inactive high to active low) serves as wake up event, thus allowing an external application to almost immediately terminate power saving. After RTS0 assertion, the CTS0 line signals module wake up, i.e., readiness of the AT command interface. It is therefore recommended to enable RTS/CTS flow control (default setting).

Figure 48 shows the described RTS0 wake up mechanism.

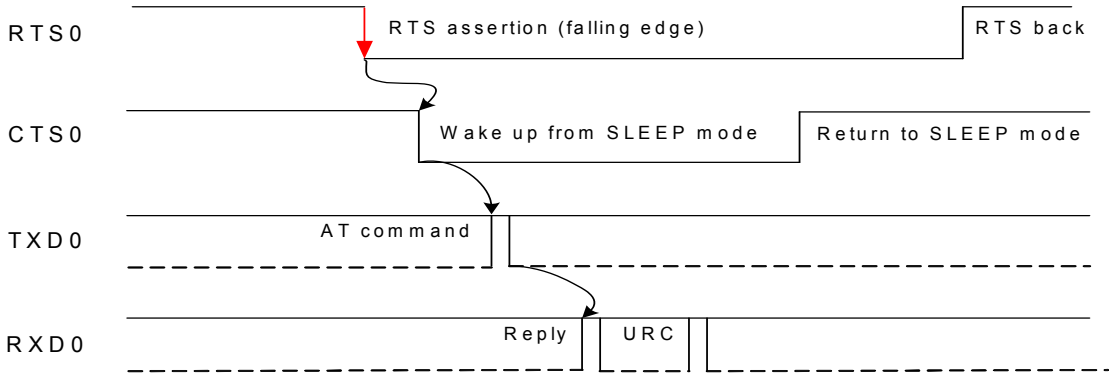



**Figure 48:** Wake-up via RTS0

## 3.5 Power Supply

ELS61-E R2 needs to be connected to a power supply at the SMT application interface - 2 lines BATT+, and GND. There are two separate voltage domains for BATT+:

- $BATT+_{BB}$ with a line mainly for the baseband power supply.
- $BATT+_{RF}$ with a line for the GSM/UMTS/LTE power amplifier supply.

Please note that throughout the document BATT+ refers to both voltage domains and power supply lines - $BATT+_{BB}$ and $BATT+_{RF}$.

The power supply of ELS61-E R2 has to be a single voltage source at $BATT+_{BB}$ and $BATT+_{RF}$. It must be able to provide the peak current during the uplink transmission.

All the key functions for supplying power to the device are handled by the power management section of the analog controller. This IC provides the following features:

- Stabilizes the supply voltages for the baseband using low drop linear voltage regulators and a DC-DC step down switching regulator.
- Switches the module's power voltages for the power-up and -down procedures.
- SIM switch to provide SIM power supply.

### 3.5.1 Power Supply Ratings

Table 17 and Table 18 assemble various voltage supply and current consumption ratings of the module.

**Table 17:** Voltage supply ratings

| | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| BATT+ | Supply voltage | Directly measured at Module. Voltage must stay within the min/max values, including voltage drop, ripple, spikes. | 3.0 | | 4.5 | V |
| | Maximum allowed voltage drop during transmit burst | Normal condition, power control level for Pout max | | | 400 | mV |
| | Voltage ripple | Normal condition, power control level for Pout max<br>@ f <= 250 kHz<br>@ f > 250 kHz | | | <br>60<br>20 | <br>$mV_{pp}$<br>$mV_{pp}$ |

**Table 18:** Current consumption ratings[1]

| | Description | Conditions | | Typical rating | Unit |
|---|---|---|---|---|---|
| $I_{VDDLP}$ @ 1.8V | OFF State supply current | RTC backup @ BATT+ = 0V | | 1.54 | µA |
| $I_{BATT+}$[2] (i.e., sum of $BATT+_{BB}$ and $BATT+_{RF}$) | OFF State supply current | Power Down | | 100 | µA |
| | Average GSM supply current | SLEEP[3] @ DRX=9 (UART deactivated) | USB disconnected | 1.8 | mA |
| | | | USB suspended | 1.8 | mA |
| | | SLEEP[3] @ DRX=5 (UART deactivated) | USB disconnected | 1.9 | mA |
| | | | USB suspended | 1.9 | mA |
| | | SLEEP[3] @ DRX=2 (UART deactivated) | USB disconnected | 2.4 | mA |
| | | | USB suspended | 2.4 | mA |
| | | IDLE[4] @ DRX=2 (UART activated, but no communication) | USB disconnected | 13 | mA |
| | | | USB active | 32 | mA |
| | | Voice Call GSM900; PCL=5 | | 275 | mA |
| | | GPRS Data transfer GSM900; PCL=5; 1Tx/ 4Rx | ROPR=4 (max. reduction) | 275 | mA |
| | | | ROPR=0 (no reduction) | 275 | |
| | | GPRS Data transfer GSM900; PCL=5; 2Tx/ 3Rx | ROPR=4 (max. reduction) | 385 | mA |
| | | | ROPR=0 (no reduction) | 525 | mA |
| | | GPRS Data transfer GSM900; PCL=5; 4Tx/ 1Rx | ROPR=4 (max. reduction) | 530 | mA |
| | | | ROPR=0 (no reduction) | 1000 | mA |
| | | EDGE Data transfer GSM900; PCL=5; 1Tx/ 4Rx | ROPR=4 (max. reduction) | 170 | mA |
| | | | ROPR=0 (no reduction) | 170 | |
| | | EDGE Data transfer GSM900; PCL=5; 2Tx/ 3Rx | ROPR=4 (max. reduction) | 250 | mA |
| | | | ROPR=0 (no reduction) | 300 | mA |
| | | EDGE Data transfer GSM900; PCL=5; 4Tx/ 1Rx | ROPR=4 (max. reduction) | 350 | mA |
| | | | ROPR=0 (no reduction) | 560 | mA |

**Table 18:** Current consumption ratings[1]

| | Description | Conditions | | Typical rating | Unit |
|---|---|---|---|---|---|
| $I_{BATT+}$[2] (i.e., sum of $BATT+_{BB}$ and $BATT+_{RF}$) | Average GSM supply current | Voice Call GSM1800; PCL=0 | | 150 | mA |
| | | GPRS Data transfer GSM1800; PCL=0; 1Tx/4Rx | ROPR=4 (max. reduction) | 150 | mA |
| | | | ROPR=0 (no reduction) | 150 | |
| | | GPRS Data transfer GSM1800; PCL=0; 2Tx/3Rx | ROPR=4 (max. reduction) | 210 | mA |
| | | | ROPR=0 (no reduction) | 270 | mA |
| | | GPRS Data transfer GSM1800; PCL=0; 4Tx/1Rx | ROPR=4 (max. reduction) | 280 | mA |
| | | | ROPR=0 (no reduction) | 475 | mA |
| | | EDGE Data transfer GSM1800; PCL=0; 1Tx/4Rx | ROPR=4 (max. reduction) | 125 | mA |
| | | | ROPR=0 (no reduction) | 120 | mA |
| | | EDGE Data transfer GSM1800; PCL=0; 2Tx/3Rx | ROPR=4 (max. reduction) | 180 | mA |
| | | | ROPR=0 (no reduction) | 210 | mA |
| | | EDGE Data transfer GSM1800; PCL=0; 4Tx/1Rx | ROPR=4 (max. reduction) | 250 | mA |
| | | | ROPR=0 (no reduction) | 365 | mA |
| | Peak current Data transfer during GSM transmit burst | GPRS Data transfer GSM900; PCL=5; 4Tx/1Rx | | 2.4 | A |
| | | GPRS Data transfer GSM1800; PCL=0; 4Tx/1Rx | | 1.2 | A |
| | Average UMTS supply current<br><br>Data transfer @ maximum Pout | SLEEP[3] @ DRX=9 (UART deactivated) | USB disconnected | 1.7 | mA |
| | | | USB suspended | 1.7 | mA |
| | | SLEEP[3] @ DRX=8 (UART deactivated) | USB disconnected | 1.7 | mA |
| | | | USB suspended | 1.7 | mA |
| | | SLEEP[3] @ DRX=6 (UART deactivated) | USB disconnected | 2.4 | mA |
| | | | USB suspended | 2.3 | mA |
| | | IDLE[4] @ DRX=6 (UART active, but no communication) | USB disconnected | 13 | mA |
| | | | USB active | 32 | mA |
| | | Voice call Band I | | 575 | mA |
| | | Voice call Band VIII | | 590 | mA |
| | | UMTS Data transfer Band I | | 560 | mA |
| | | UMTS Data transfer Band VIII | | 570 | mA |
| | | HSPA Data transfer Band I | | 595 | mA |
| | | HSPA Data transfer Band VIII | | 590 | mA |

**Table 18:** Current consumption ratings[1]

| | Description | Conditions | | Typical rating | Unit |
|---|---|---|---|---|---|
| $I_{BATT+}$[2] (i.e., sum of $BATT+_{BB}$ and $BATT+_{RF}$) | Average LTE supply current<br><br>Data transfer @ maximum Pout | SLEEP[3] @ "Paging Occasions" = 256 | USB disconnected | 1.6 | mA |
| | | | USB suspended | 1.6 | mA |
| | | SLEEP[3] @ "Paging Occasions" = 128 | USB disconnected | 2.0 | mA |
| | | | USB suspended | 2.0 | mA |
| | | SLEEP[3] @ "Paging Occasions" = 64 | USB disconnected | 2.7 | mA |
| | | | USB suspended | 2.7 | mA |
| | | SLEEP[3] @ "Paging Occasions" = 32 | USB disconnected | 4.3 | mA |
| | | | USB suspended | 4.3 | mA |
| | | IDLE[4] @ DRX=6 (UART active, but no communication) | USB disconnected | 15 | mA |
| | | | USB active | 35 | mA |
| | | LTE[5] Data transfer Band 1 | | 625 | mA |
| | | LTE[5] Data transfer Band 3 | | 670 | mA |
| | | LTE[5] Data transfer Band 8 | | 630 | mA |
| | | LTE[5] Data transfer Band 20 | | 560 | mA |
| | | LTE[5] Data transfer Band 28 | | 570 | mA |

1. Note: Current consumption ratings are based on measurements done in a laboratory test environment and deviations may occur from the given typical rating. Under real life conditions however, with e.g., varying network quality, location changes, or changing supply currents, the deviation from these typical ratings may be even bigger, and will have to be taken into account for actual power supply solutions. For more details on power supply design see [3].
2. With an impedance of $Z_{LOAD}$=50Ω at the antenna pad.Measured at 25°C and 3.8V.
3. Measurements start 6 minutes after switching ON the module;
Averaging times: SLEEP mode - 3 minutes, transfer modes - 1.5 minutes
Communication tester settings: No neighbor cells, no cell re-selection etc., RMC (reference measurement channel). Note that SLEEP mode is enabled via AT Command AT^SPOW=2,1000,3
4. The power saving mode is disabled via AT command AT^SPOW=1,0,0
5. Communication tester settings:
Channel Bandwidth: 5MHz
Number of Resource Blocks: 25 (DL), 1 (UL)
Modulation: QPSK

### 3.5.2 Minimizing Power Losses

When designing the power supply for your application please pay specific attention to power losses. Ensure that the input voltage $V_{BATT+}$ never drops below 3.0V on the ELS61-E R2 board, not even in a GSM transmit burst where current consumption can rise (for peak values see the power supply ratings listed in Section 3.5.1).

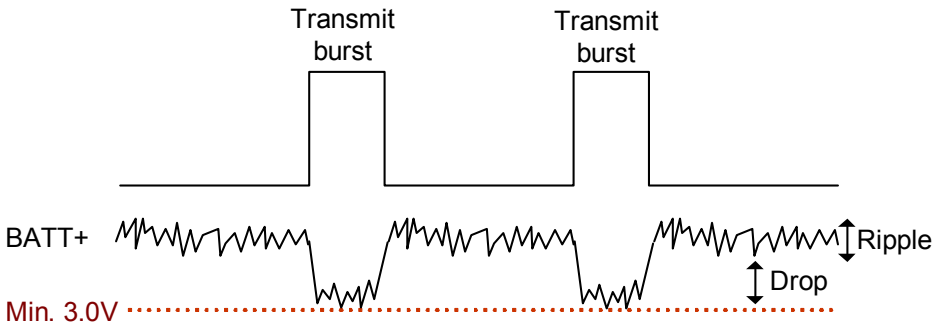



**Figure 49:** Power supply limits during transmit burst

### 3.5.3 Measuring the Supply Voltage ($V_{BATT+}$)

To measure the supply voltage $V_{BATT+}$ it is possible to define two reference points GND and BATT+. GND should be the module's shielding, while BATT+ should be a test pad on the external application the module is mounted on. The external BATT+ reference point has to be connected to and positioned close to the SMT application interface's BATT+ pads 53 ($BATT+_{RF}$) or 204 ($BATT+_{BB}$) as shown in Figure 50.

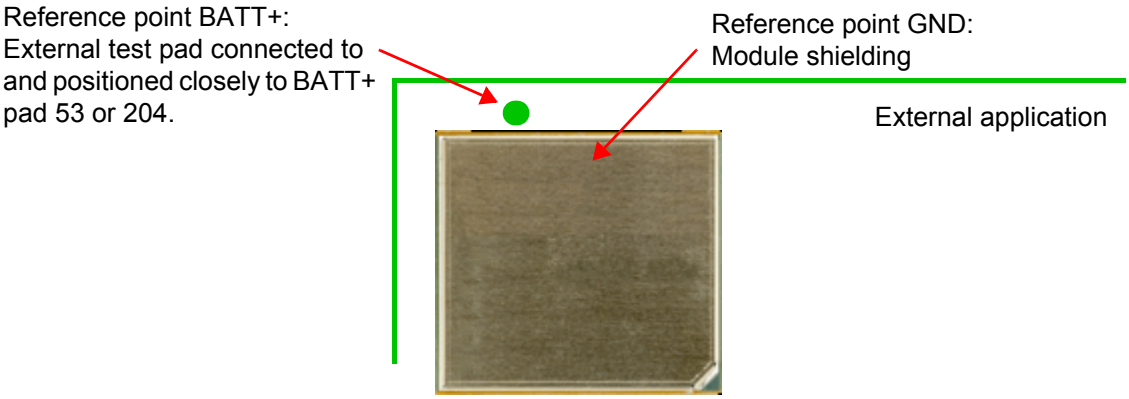



**Figure 50:** Position of reference points BATT+ and GND

### 3.5.4 Monitoring Power Supply by AT Command

To monitor the supply voltage you can also use the AT^SBV command which returns the value related to the reference points BATT+ and GND.

The module continuously measures the voltage at intervals depending on the operating mode of the RF interface. The duration of measuring ranges from 0.5 seconds in TALK/DATA mode to 50 seconds when ELS61-E R2 is in IDLE mode or Limited Service (deregistered). The displayed voltage (in mV) is averaged over the last measuring period before the AT^SBV command was executed.

If the measured voltage drops below or rises above the voltage shutdown thresholds, the module will send an "^SBC" URC and shut down (for details see Section 3.2.5).

## 3.6 Operating Temperatures

Please note that the module's lifetime, i.e., the MTTF (mean time to failure) may be reduced, if operated outside the extended temperature range.

**Table 19:** Board temperature

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Normal operation | -30 | +25 | +85 | °C |
| Extended operation[1] | -40 | | +90 | °C |
| Automatic shutdown[2]<br>Temperature measured on ELS61-E R2 board | <-40 | --- | >+90 | °C |

1. Extended operation allows normal mode speech calls or data transmission for limited time until automatic thermal shutdown takes effect. Within the extended temperature range (outside the normal operating temperature range) the specified electrical characteristics may be in- or decreased.
2. Due to temperature measurement uncertainty, a tolerance of ±3°C on the thresholds may occur.

See also Section 3.2.5 for information about the NTC for on-board temperature measurement, automatic thermal shutdown and alert messages.

Note: Within the specified operating temperature ranges the board temperature may vary to a great extent depending on operating mode, used frequency band, radio output power and current supply voltage.

For more information regarding the module's thermal behavior please refer to [5].

## 3.7 Electrostatic Discharge

The module is not protected against Electrostatic Discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates a ELS61-E R2 module.

An example for an enhanced ESD protection for the SIM interface is given in Section 2.1.6.1.

ELS61-E R2 has been tested according to group standard ETSI EN 301 489-1 (see Table 26) and test standard EN 61000-4-2. Electrostatic values can be gathered from the following table.

**Table 20:** Electrostatic values

| Specification/Requirements | Contact discharge | Air discharge |
|---|---|---|
| **EN 61000-4-2** | | |
| Antenna interfaces | ±1kV | n.a. |
| Antenna interfaces with ESD protection (see Section 3.7.1) | ±4kV | ±8kV |
| BATT+ | ±4kV | ±8kV |
| **JEDEC JESD22-A114D** (Human Body Model, Test conditions: 1.5 kΩ, 100 pF) | | |
| All other interfaces | ±1kV | n.a. |

Note: The values may vary with the individual application design. For example, it matters whether or not the application platform is grounded over external devices like a computer or other equipment, such as the Thales reference application described in Chapter 5.

### 3.7.1 ESD Protection for Antenna Interfaces

The following Figure 51 shows how to implement an external ESD protection for the RF antenna interfaces (ANT_MAIN and ANT_DRX) with either a T pad or PI pad attenuator circuit (for RF line routing design see also Section 2.2.3).

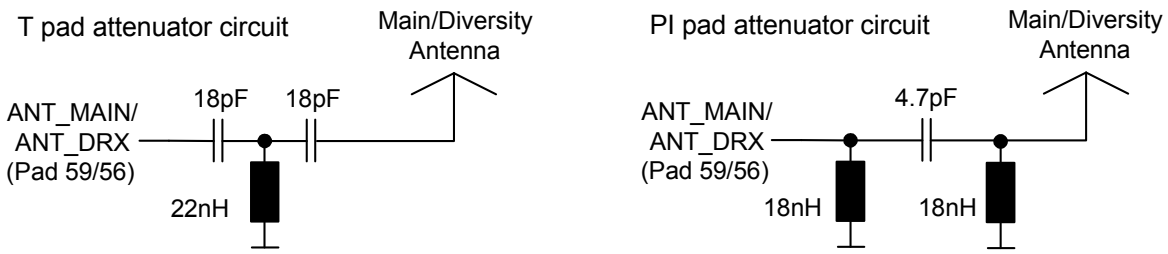



**Figure 51:** ESD protection for RF antenna interface

Recommended inductor types for the above sample circuits: Size 0402 SMD from Panasonic ELJRF series (22nH and 18nH inductors) or Murata LQW15AN18NJ00 (18nH inductors only).

## 3.8 Blocking against RF on Interface Lines

To reduce EMI issues there are serial resistors, or capacitors to GND, implemented on the module for the ignition, emergency restart, and SIM interface lines (cp. Section 2.3). However, all other signal lines have no EMI measures on the module and there are no blocking measures at the module's interface to an external application.

Dependent on the specific application design, it might be useful to implement further EMI measures on some signal lines at the interface between module and application. These measures are described below.

There are five possible variants of EMI measures (A-E) that may be implemented between module and external application depending on the signal line (see Figure 52 and Table 21). Pay attention not to exceed the maximum input voltages and prevent voltage overshots if using inductive EMC measures.

The maximum value of the serial resistor should be lower than 1kΩ on the signal line. The maximum value of the capacitor should be lower than 50pF on the signal line. Please observe the electrical specification of the module‘s SMT application interface and the external application‘s interface.

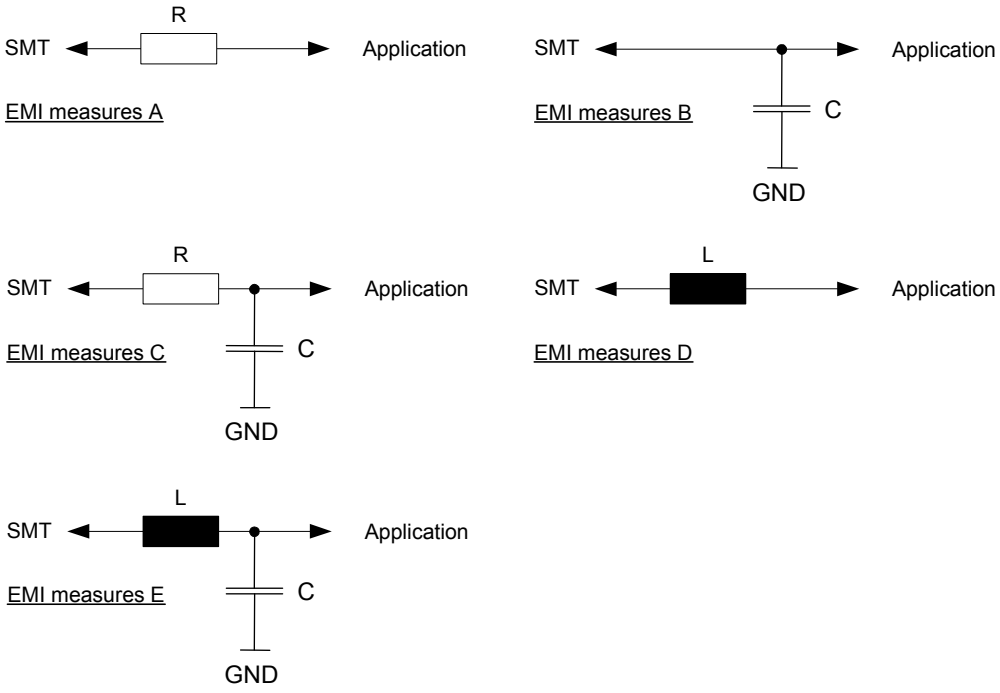



**Figure 52:** EMI circuits

Note: In case the application uses an internal RF antenna that is implemented close to the ELS61-E R2 module, Thales strongly recommends sufficient EMI measures, e.g. of type B or C, for each digital input or output.

The following table lists for each signal line at the module‘s SMT application interface the EMI measures that may be implemented.

**Table 21:** EMI measures on the application interface

| Signal name | EMI measures | | | | | Remark |
|---|---|---|---|---|---|---|
| | A | B | C | D | E | |
| CCIN | x | | | x | | |
| CCRST | | x | | | | The external capacitor should be not higher than 30pF. The value of the capacitor depends on the external application. |
| CCIO | | x | | | | |
| CCCLK | | x | | | | |
| RXD0 | x | x | x | x | x | |
| TXD0 | x | x | x | x | x | |
| CTS0 | x | x | x | x | x | |
| RTS0 | x | x | x | x | x | |
| GPIO1/DTR0 | x | x | x | x | x | |
| GPIO2/DCD0 | x | x | x | x | x | |
| GPIO3/DSR0/SPI_CLK | x | x | x | x | x | |
| GPIO4/FST_SHDN | x | x | x | x | x | |
| GPIO5/LED | x | x | x | x | x | |
| GPIO6/PWM2 | x | x | x | x | x | |
| GPIO7/PWM1 | x | x | x | x | x | |
| GPIO8/COUNTER | x | x | x | x | x | |
| GPIO11-GPIO15 | x | x | x | x | x | |
| GPIO16/RXD1/MOSI | x | x | x | x | x | |
| GPIO17/TXD1/MISO | x | x | x | x | x | |
| GPIO18/RTS1 | x | x | x | x | x | |
| GPIO19/CTS1/SPI_CS | x | x | x | x | x | |
| GPIO20/DOUT | x | x | x | x | x | |
| GPIO21/DIN | x | x | x | x | x | |
| GPIO22/FSC | x | x | x | x | x | |
| GPIO23/BCLK | x | x | x | x | x | |
| GPIO24/RING0 | x | x | x | x | x | |
| I2CDAT | | x | | x | | The rising signal edge is reduced with an additional capacitor. |
| I2CCLK | | x | | x | | |
| V180 | | x | | x | x | |
| VCORE | | x | | x | x | |
| $BATT+_{RF}$ (pad 53) | | x | x | | | Measures required if $BATT+_{RF}$ is close to internal RF antenna - e.g., 39pF blocking capacitor to ground |
| $BATT+_{BB}$ (pad 204) | | x | x | | | |
| VUSB | | x | | x | x | |
| USB_DP | | | | | | It is not allowed to use any external ESD or EMI components at this interface signal lines. |
| USB_DN | | | | | | |

## 3.9 Reliability Characteristics

The test conditions stated below are an extract of the complete test specifications.

**Table 22:** Summary of reliability test conditions

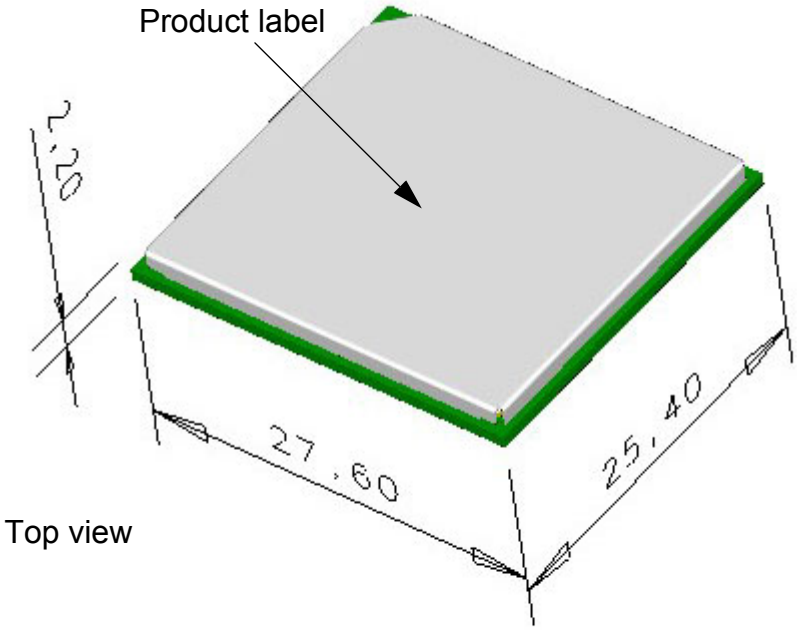
| Type of test | Conditions | Standard |
|---|---|---|
| Vibration | Frequency range: 10-20Hz; acceleration: 5g<br>Frequency range: 20-500Hz; acceleration: 20g<br>Duration: 20h per axis; 3 axes | DIN IEC 60068-2-6[1] |
| Shock half-sinus | Acceleration: 500g<br>Shock duration: 1ms<br>1 shock per axis<br>6 positions (± x, y and z) | DIN IEC 60068-2-27 |
| Dry heat | Temperature: +70 ±2°C<br>Test duration: 16h<br>Humidity in the test chamber: < 50% | EN 60068-2-2 Bb<br>ETS 300 019-2-7 |
| Temperature change (shock) | Low temperature: -40°C ±2°C<br>High temperature: +85°C ±2°C<br>Changeover time: < 30s (dual chamber system)<br>Test duration: 1h<br>Number of repetitions: 100 | DIN IEC 60068-2-14 Na<br><br>ETS 300 019-2-7 |
| Damp heat cyclic | High temperature: +55°C ±2°C<br>Low temperature: +25°C ±2°C<br>Humidity: 93% ±3%<br>Number of repetitions: 6<br>Test duration: 12h + 12h | DIN IEC 60068-2-30 Db<br><br>ETS 300 019-2-5 |
| Cold (constant exposure) | Temperature: -40 ±2°C<br>Test duration: 16h | DIN IEC 60068-2-1 |

1. For reliability tests in the frequency range 20-500Hz the Standard's acceleration reference value was increased to 20g.

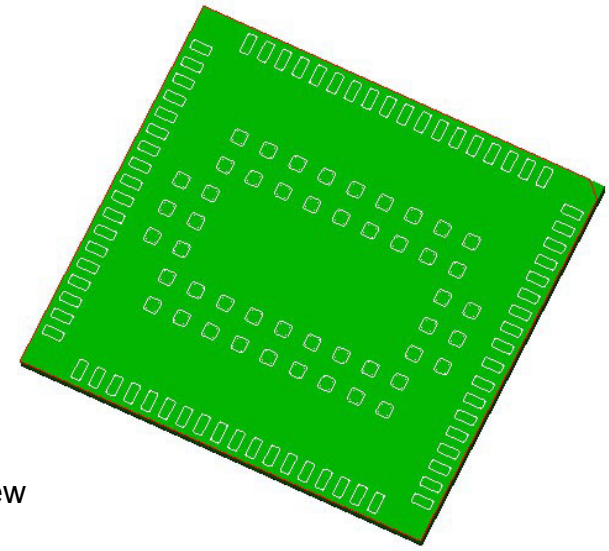
# 4 Mechanical Dimensions, Mounting and Packaging

## 4.1 Mechanical Dimensions of ELS61-E R2

Figure 53 shows the top and bottom view of ELS61-E R2 and provides an overview of the board's mechanical dimensions. For further details see Figure 54.




Top view



Bottom view

**Figure 53:** ELS61-E R2– top and bottom view

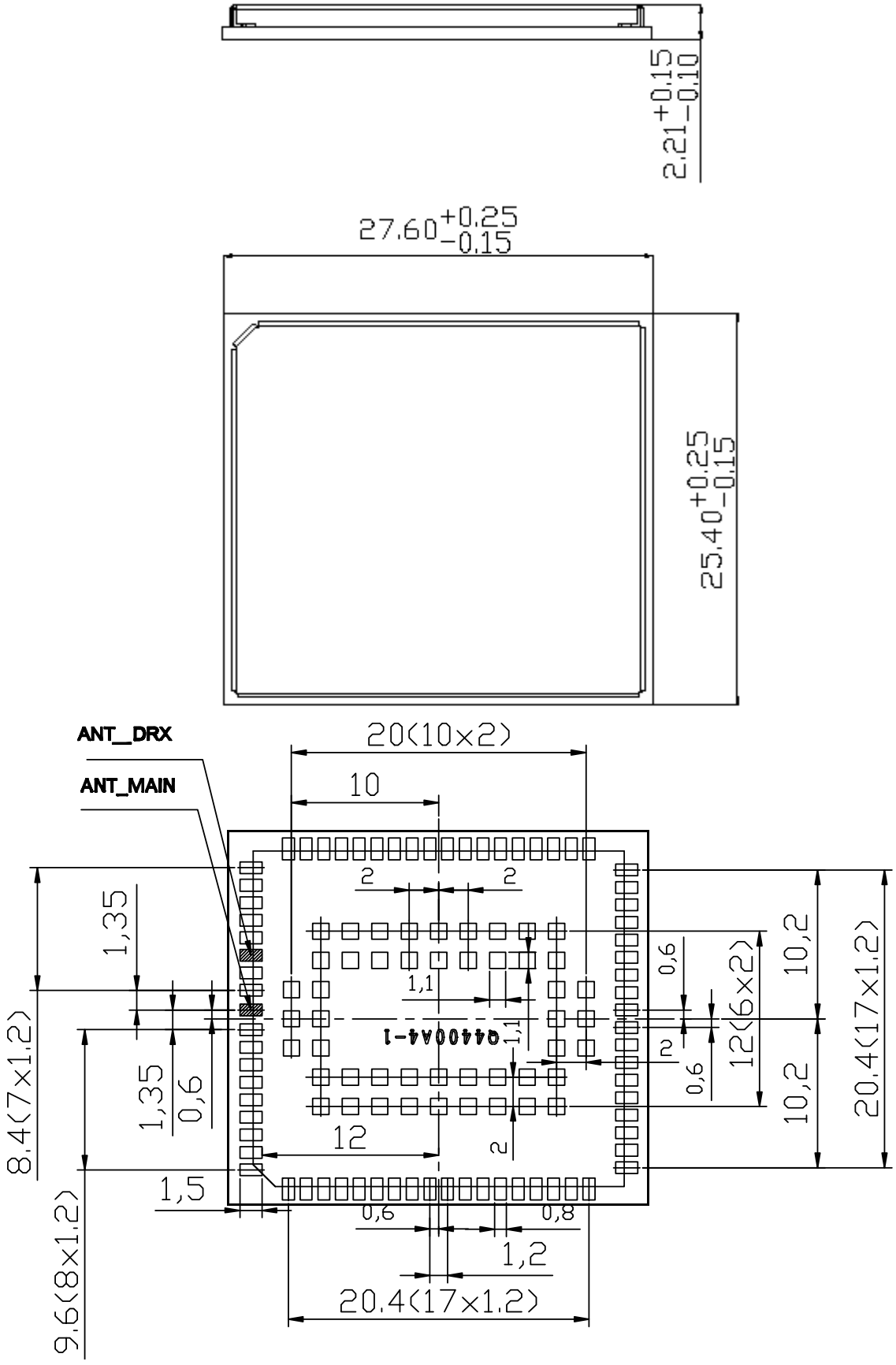



**Figure 54:** Dimensions of ELS61-E R2 (all dimensions in mm)

## 4.2 Mounting ELS61-E R2 onto the Application Platform

This section describes how to mount ELS61-E R2 onto the PCBs, including land pattern and stencil design, board-level characterization, soldering conditions, durability and mechanical handling. For more information on issues related to SMT module integration see also [4].

Note: To avoid short circuits between signal tracks on an external application's PCB and various markings at the bottom side of the module, it is recommended not to route the signal tracks on the top layer of an external PCB directly under the module, or at least to ensure that signal track routes are sufficiently covered with solder resist.

### 4.2.1 SMT PCB Assembly

#### 4.2.1.1 Land Pattern and Stencil

The land pattern and stencil design as shown below is based on Thales characterizations for lead-free solder paste on a four-layer test PCB and a respectively 110 µm and 150 µm thick stencil.

The land pattern given in Figure 55 reflects the module‘s pad layout, including signal pads and ground pads (for pad assignment see Section 2.1.1).

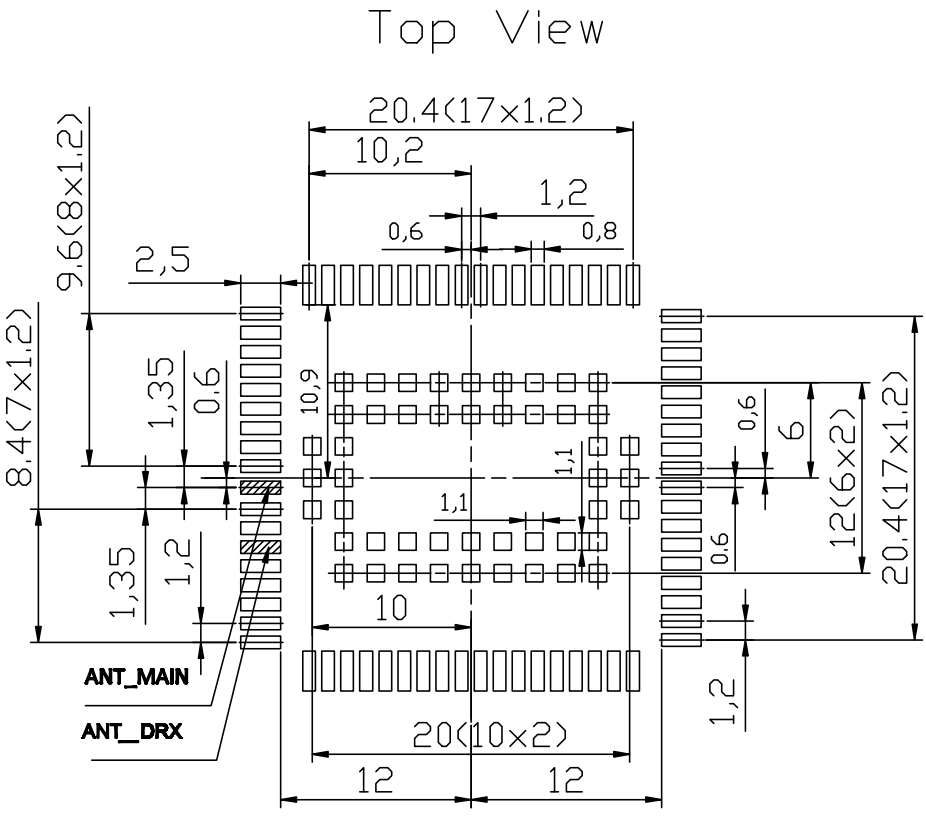



**Figure 55:** Land pattern (top view)

The stencil design illustrated in Figure 56 and Figure 57 is recommended by Thales as a result of extensive tests with Thales Daisy Chain modules.

The central ground pads are primarily intended for stabilizing purposes, and may show some more voids than the application interface pads at the module's rim. This is acceptable, since they are electrically irrelevant.

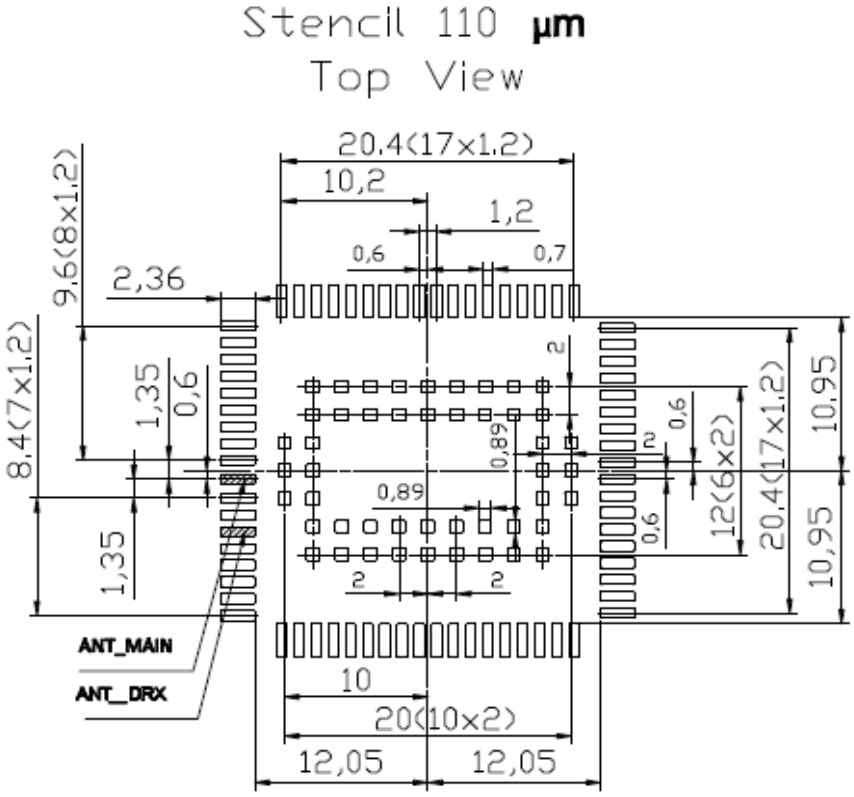



**Figure 56:** Recommended design for 110µm thick stencil (top view)

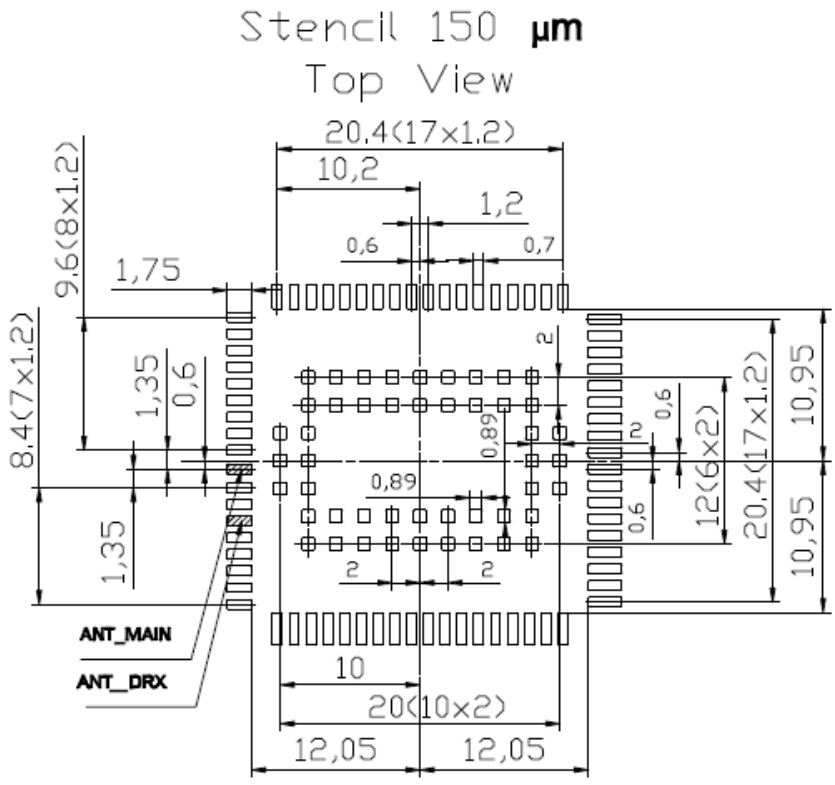



**Figure 57:** Recommended design for 150µm thick stencil (top view)

#### 4.2.1.2 Board Level Characterization

Board level characterization issues should also be taken into account if devising an SMT process.

Characterization tests should attempt to optimize the SMT process with regard to board level reliability. This can be done by performing the following physical tests on sample boards: Peel test, bend test, tensile pull test, drop shock test and temperature cycling. Sample surface mount checks are described in [4].

It is recommended to characterize land patterns before an actual PCB production, taking individual processes, materials, equipment, stencil design, and reflow profile into account. For land and stencil pattern design recommendations see also Section 4.2.1.1. Optimizing the solder stencil pattern design and print process is necessary to ensure print uniformity, to decrease solder voids, and to increase board level reliability.

Daisy chain modules for SMT characterization are available on request. For details refer to [4].

Generally, solder paste manufacturer recommendations for screen printing process parameters and reflow profile conditions should be followed. Maximum ratings are described in Section 4.2.3.

### 4.2.2 Moisture Sensitivity Level

ELS61-E R2 comprises components that are susceptible to damage induced by absorbed moisture.

Thales' ELS61-E R2 module complies with the latest revision of the IPC/JEDEC J-STD-020 Standard for moisture sensitive surface mount devices and is classified as MSL 4.

For additional moisture sensitivity level (MSL) related information see Section 4.2.4 and Section 4.3.2.

## 4.2.3 Soldering Conditions and Temperature

### 4.2.3.1 Reflow Profile

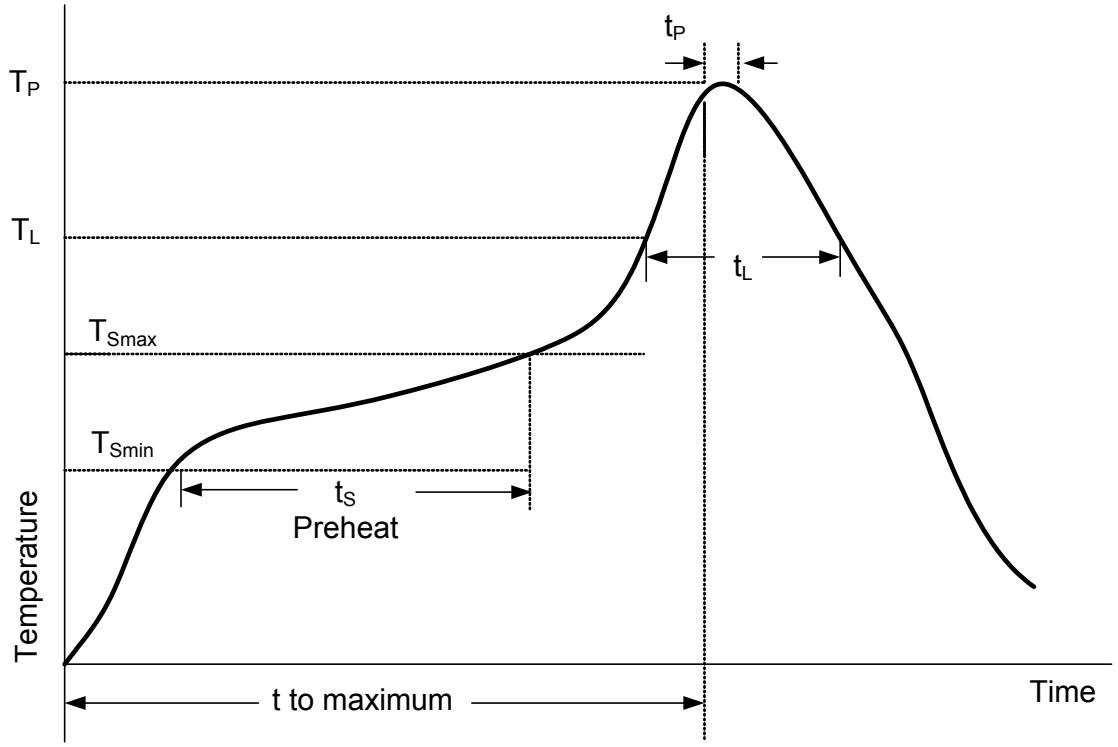
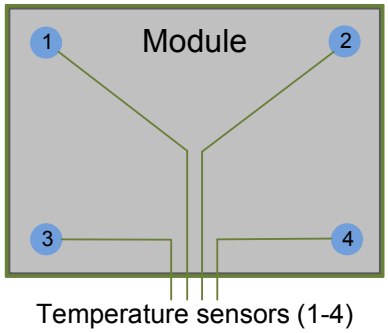



**Figure 58:** Reflow Profile

**Table 23:** Reflow temperature ratings[1]

| Profile Feature | Pb-Free Assembly |
|---|---|
| Preheat & Soak<br>Temperature Minimum ($T_{Smin}$)<br>Temperature Maximum ($T_{Smax}$)<br>Time ($t_{Smin}$ to $t_{Smax}$) ($t_S$) | <br>150°C<br>200°C<br>60-120 seconds |
| Average ramp up rate ($T_L$ to $T_P$) | 3K/second max. [2] |
| Liquidous temperature ($T_L$)<br>Time at liquidous ($t_L$) | 217°C<br>50-90 seconds |
| Peak package body temperature ($T_P$) | 245°C +0/-5°C |
| Time ($t_P$) within 5 °C of the peak package body temperature ($T_P$) | 30 seconds max. |
| Average ramp-down rate | 3 K/second max. [2] |
| Time 25°C to maximum temperature | 8 minutes max. |

1. Please note that the reflow profile features and ratings listed above are based on the joint industry standard IPC/JEDEC J-STD-020D.1, and are as such meant as a general guideline. For more information on reflow profiles and their optimization please refer to [4].
2. Temperatures measured on shielding at each corner. See also [4].




### 4.2.3.2 Maximum Temperature and Duration

The following limits are recommended for the SMT board-level soldering process to attach the module:

- A maximum module temperature of 245°C. This specifies the temperature as measured at the module's top side.
- A maximum duration of 30 seconds at this temperature.

Please note that while the solder paste manufacturers' recommendations for best temperature and duration for solder reflow should generally be followed, the limits listed above must not be exceeded.

ELS61-E R2 is specified for one soldering cycle only. Once ELS61-ER2 is removed from the application, the module will very likely be destroyed and cannot be soldered onto another application.

## 4.2.4 Durability and Mechanical Handling

### 4.2.4.1 Storage Conditions

ELS61-E R2 modules, as delivered in tape and reel carriers, must be stored in sealed, moisture barrier anti-static bags. The conditions stated below are only valid for modules in their original packed state in weather protected, non-temperature-controlled storage locations. Normal storage time under these conditions is 12 months maximum.

**Table 24:** Storage conditions

| Type | Condition | Unit | Reference |
|---|---|---|---|
| Air temperature: Low<br>High | -25<br>+40 | °C | IPC/JEDEC J-STD-033A |
| Humidity relative: Low<br>High | 10<br>90 at 40°C | % | IPC/JEDEC J-STD-033A |
| Air pressure: Low<br>High | 70<br>106 | kPa | IEC TR 60271-3-1: 1K4<br>IEC TR 60271-3-1: 1K4 |
| Movement of surrounding air | 1.0 | m/s | IEC TR 60271-3-1: 1K4 |
| Water: rain, dripping, icing and frosting | Not allowed | --- | --- |
| Radiation: Solar<br>Heat | 1120<br>600 | $W/m^2$ | ETS 300 019-2-1: T1.2, IEC 60068-2-2 Bb<br>ETS 300 019-2-1: T1.2, IEC 60068-2-2 Bb |
| Chemically active substances | Not recommended | | IEC TR 60271-3-1: 1C1L |
| Mechanically active substances | Not recommended | | IEC TR 60271-3-1: 1S1 |
| Vibration sinusoidal:<br>Displacement<br>Acceleration<br>Frequency range | <br>1.5<br>5<br>2-9 9-200 | <br>mm<br>$m/s^2$<br>Hz | IEC TR 60271-3-1: 1M2 |
| Shocks:<br>Shock spectrum<br>Duration<br>Acceleration | <br>semi-sinusoidal<br>1<br>50 | <br><br>ms<br>$m/s^2$ | IEC 60068-2-27 Ea |

### 4.2.4.2 Processing Life

ELS61-E R2 must be soldered to an application within 72 hours after opening the moisture barrier bag (MBB) it was stored in.

As specified in the IPC/JEDEC J-STD-033 Standard, the manufacturing site processing the modules should have ambient temperatures below 30°C and a relative humidity below 60%.

### 4.2.4.3 Baking

Baking conditions are specified on the moisture sensitivity label attached to each MBB (see Figure 63 for details):

- It is *not necessary* to bake ELS61-E R2, if the conditions specified in Section 4.2.4.1 and Section 4.2.4.2 were not exceeded.
- It is *necessary* to bake ELS61-E R2, if any condition specified in Section 4.2.4.1 and Section 4.2.4.2 was exceeded.

If baking is necessary, the modules must be put into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature.

### 4.2.4.4 Electrostatic Discharge

Electrostatic discharge (ESD) may lead to irreversable damage for the module. It is therefore advisable to develop measures and methods to counter ESD and to use these to control the electrostatic environment at manufacturing sites.

Please refer to Section 3.7 for further information on electrostatic discharge.

# 4.3 Packaging

## 4.3.1 Tape and Reel

The single-feed tape carrier for ELS61-E R2 is illustrated in Figure 59. The figure also shows the proper part orientation. The tape width is 44mm and the ELS61-ER2 modules are placed on the tape with a 32-mm pitch. The reels are 330mm in diameter with a core diameter of 100mm. Each reel contains 500 modules.

### 4.3.1.1 Orientation

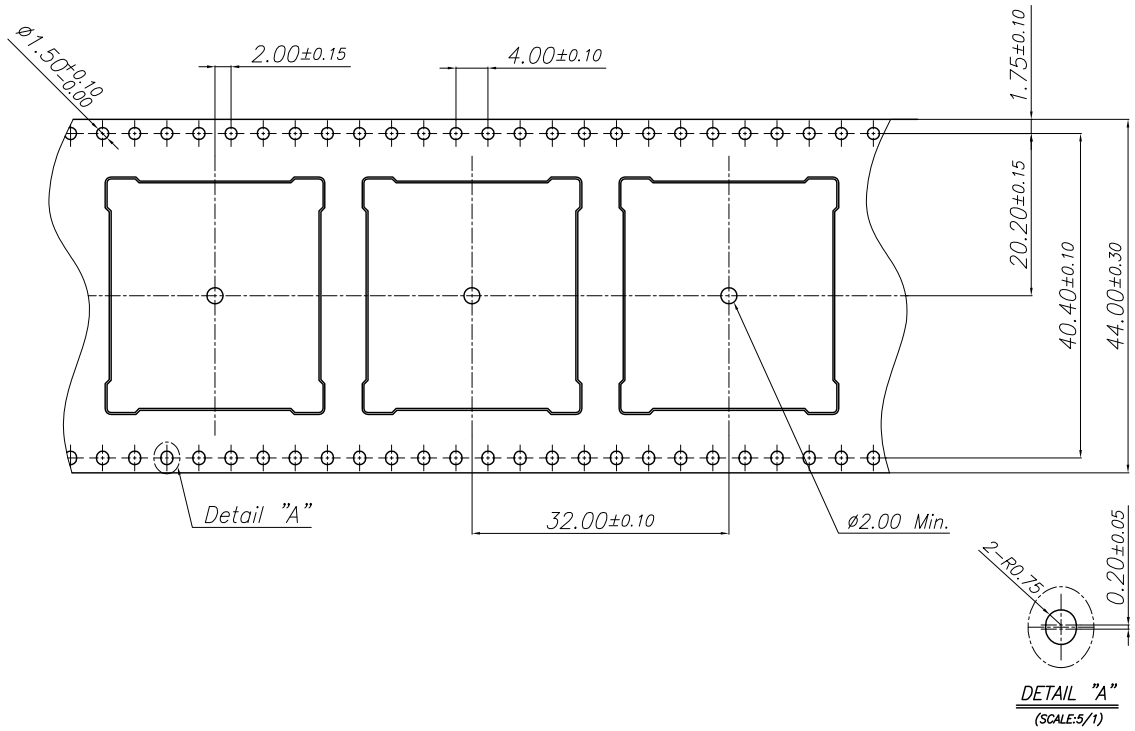



**Figure 59:** Carrier tape

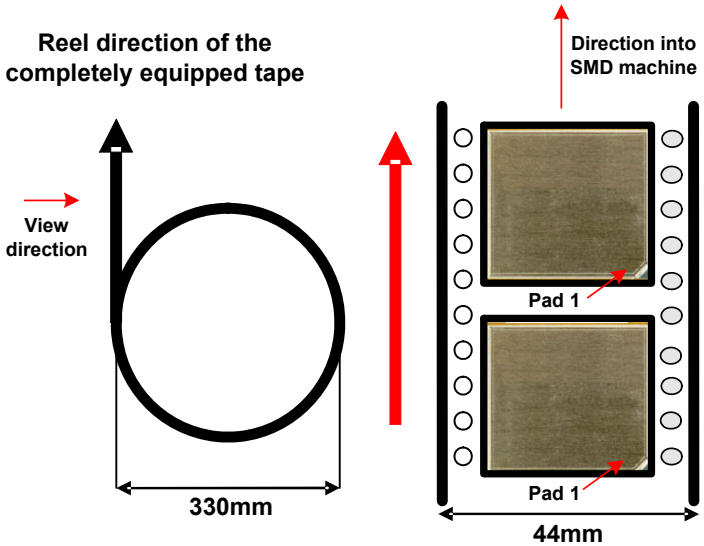



**Figure 60:** Reel direction

### 4.3.1.2 Barcode Label

A barcode label provides detailed information on the tape and its contents. It is attached to the reel.

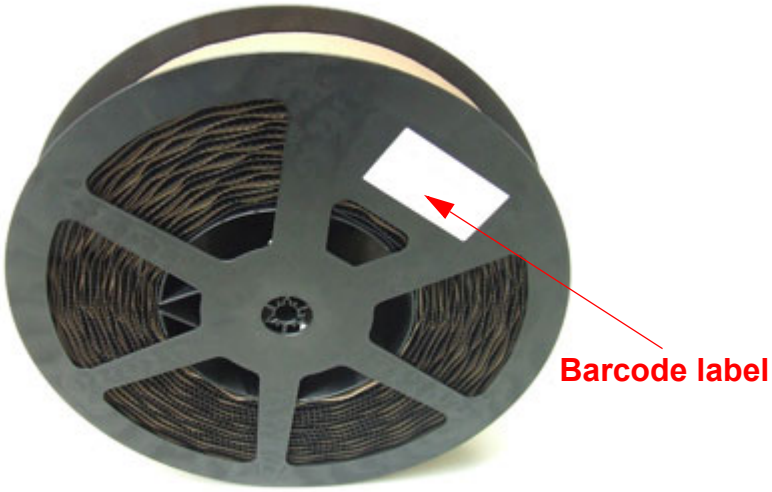



**Figure 61:** Barcode label on tape reel

### 4.3.2 Shipping Materials

ELS61-E R2 is distributed in tape and reel carriers. The tape and reel carriers used to distribute ELS61-E R2 are packed as described below, including the following required shipping materials:

- Moisture barrier bag, including desiccant and humidity indicator card
- Transportation box

#### 4.3.2.1 Moisture Barrier Bag

The tape reels are stored inside a moisture barrier bag (MBB), together with a humidity indicator card and desiccant pouches - see Figure 62. The bag is ESD protected and delimits moisture transmission. It is vacuum-sealed and should be handled carefully to avoid puncturing or tearing. The bag protects the ELS61-E R2 modules from moisture exposure. It should not be opened until the devices are ready to be soldered onto the application.

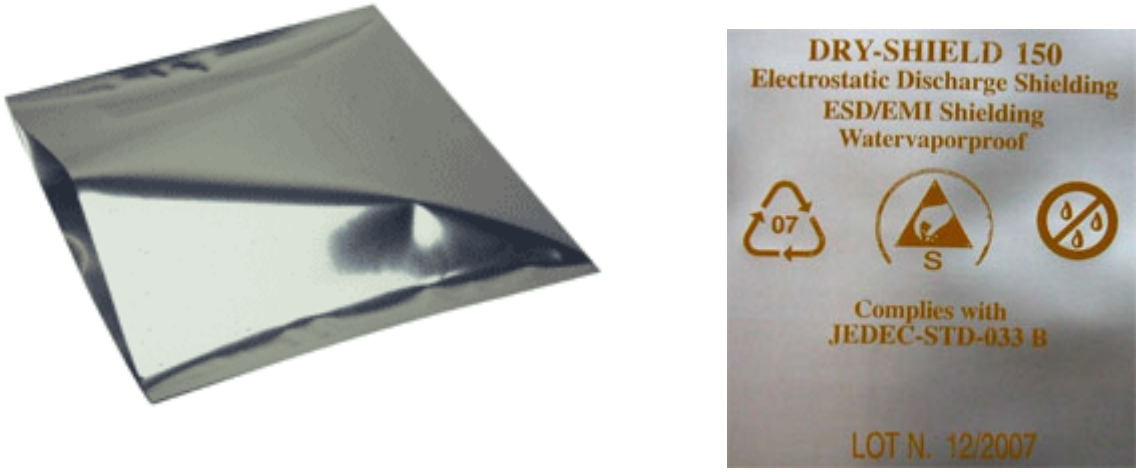



**Figure 62:** Moisture barrier bag (MBB) with imprint

The label shown in Figure 63 summarizes requirements regarding moisture sensitivity, including shelf life and baking requirements. It is attached to the outside of the moisture barrier bag.

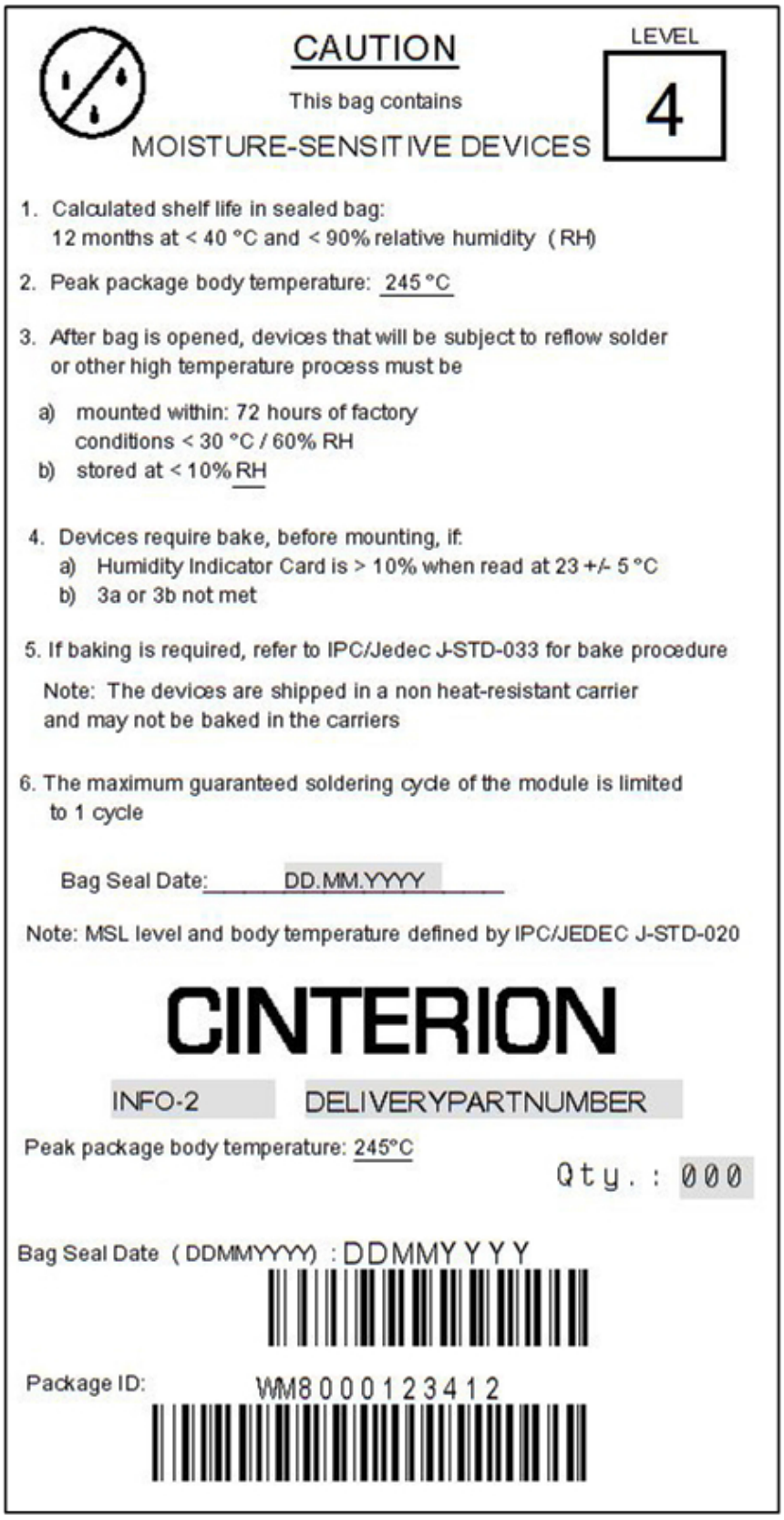



**Figure 63:** Moisture Sensitivity Label

MBBs contain one or more desiccant pouches to absorb moisture that may be in the bag. The humidity indicator card described below should be used to determine whether the enclosed components have absorbed an excessive amount of moisture.

The desiccant pouches should not be baked or reused once removed from the MBB.

The humidity indicator card is a moisture indicator and is included in the MBB to show the approximate relative humidity level within the bag. Sample humidity cards are shown in Figure 64. If the components have been exposed to moisture above the recommended limits, the units will have to be rebaked.

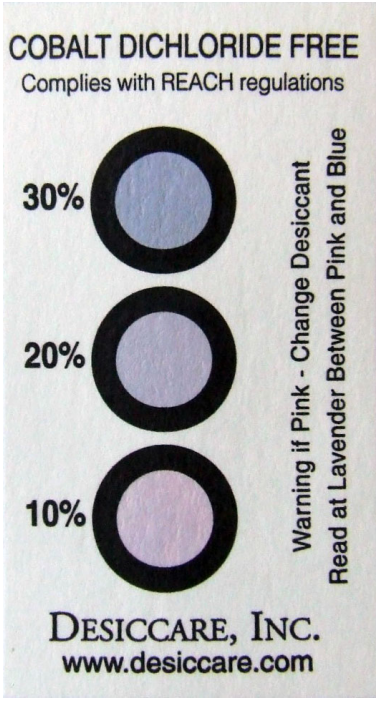



**Figure 64:** Humidity Indicator Card - HIC

A baking is required if the humidity indicator inside the bag indicates 10% RH or more.

### 4.3.2.2 Transportation Box

Tape and reel carriers are distributed in a box, marked with a barcode label for identification purposes. A box contains two reels with 500 modules each.

### 4.3.3 Trays

If small module quantities are required, e.g., for test and evaluation purposes, ELS61-E R2 may be distributed in trays (for dimensions see Figure 65). The small quantity trays are an alternative to the single-feed tape carriers normally used. However, the trays are not designed for machine processing. They contain modules to be (hand) soldered onto an external application (for information on hand soldering see [4]).

Trays are packed and shipped in the same way as tape carriers, including a moisture barrier bag with desiccant and humidity indicator card as well as a transportation box (see also Section 4.3.2).

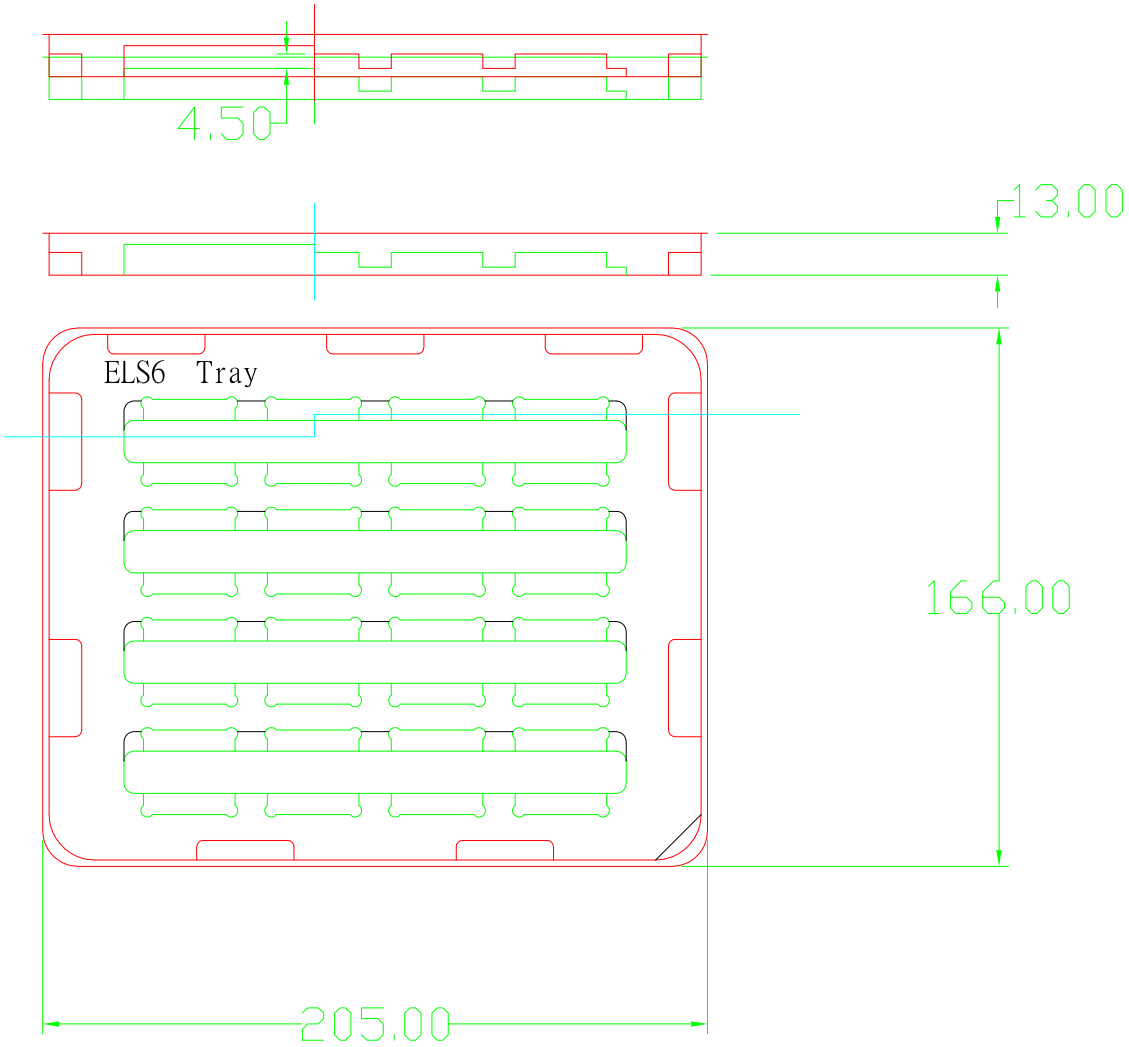



**Figure 65:** Tray dimensions

# 5 Regulatory and Type Approval Information

## 5.1 Directives and Standards

ELS61-E R2 is designed to comply with the directives and standards listed below.

It is the responsibility of the application manufacturer to ensure compliance of the final product with all provisions of the applicable directives and standards as well as with the technical specifications provided in the "ELS61-E R2 Hardware Interface Description".[1]

**Table 25:** Directives

| | |
|---|---|
| 2014/53/EU | Directive of the European Parliament and of the council of 16 April 2014 on the harmonization of the laws of the Member States relating to the making available on the market of radio equipment and repealing Directive 1999/05/EC.<br><br>The product is labeled with the CE conformity mark. |
| 2002/95/EC (RoHS 1)<br>2011/65/EC (RoHS 2) | Directive of the European Parliament and of the Council of 27 January 2003 (and revised on 8 June 2011) on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS) |

**Table 26:** Standards of European type approval

| | |
|---|---|
| 3GPP TS 51.010-1 | Digital cellular telecommunications system (Release 9); Mobile Station (MS) conformance specification; |
| GCF-CC V3.67 | Global Certification Forum - Certification Criteria |
| ETSI EN 301 511 V12.5.1 | Global System for Mobile communications (GSM); Mobile Stations (MS) equipment; Harmonized Standard covering the essential requirements of article 3.2 of Directive 2014/53/EU |
| Draft ETSI EN 301 489-01 V2.2.0 | Electromagnetic Compatibility (EMC) standard for radio equipment and services; Part 1: Common technical requirements; Harmonized Standard covering the essential requirements of article 3.1(b) of Directive 2014/53/EU and the essential requirements of article 6 of Directive 2014/30/EU |
| Draft ETSI EN 301 489-52 V1.1.0 | Electromagnetic Compatibility (EMC) standard for radio equipment and services; Part 52: Specific conditions for Cellular Communication Mobile and portable (UE) radio and ancillary equipment; Harmonized Standard covering the essential requirements of article 3.1(b) of Directive 2014/53/EU |
| ETSI EN 301 908-1 V11.1.1 | IMT cellular networks; Harmonized Standard covering the essential requirements of article 3.2 of the Directive 2014/53/EU; Part 1: Introduction and common requirements |
| ETSI EN 301 908-2 V11.1.2 | IMT cellular networks; Harmonized Standard covering the essential requirements of article 3.2 of the Directive 2014/53/EU; Part 2: CDMA Direct Spread (UTRA FDD) User Equipment (UE) |

1. Manufacturers of applications which can be used in the US shall ensure that their applications have a PTCRB approval. For this purpose they can refer to the PTCRB approval of the respective module.

**Table 26:** Standards of European type approval

| | |
|---|---|
| ETSI EN 301 908-13 V11.1.2 | IMT cellular networks; Harmonized Standard covering the essential requirements of article 3.2 of the Directive 2014/53/EU; Part 13: Evolved Universal Terrestrial Radio Access (E-UTRA) User Equipment (UE) |
| EN 60950-1: 2006 +A11:2009+A1:2010+A 12:2011+A2:2013 | Safety of information technology equipment |

**Table 27:** Requirements of quality

| | |
|---|---|
| IEC 60068 | Environmental testing |
| DIN EN 60529 | IP codes |

**Table 28:** Standards of the Ministry of Information Industry of the People's Republic of China

| | |
|---|---|
| SJ/T 11363-2006 | "Requirements for Concentration Limits for Certain Hazardous Substances in Electronic Information Products" (2006-06). |
| SJ/T 11364-2006 | "Marking for Control of Pollution Caused by Electronic Information Products" (2006-06).<br><br>According to the "Chinese Administration on the Control of Pollution caused by Electronic Information Products" (ACPEIP) the EPUP, i.e., Environmental Protection Use Period, of this product is 20 years as per the symbol shown here, unless otherwise marked. The EPUP is valid only as long as the product is operated within the operating limits described in the Thales Hardware Interface Description.<br><br>Please see Table 29 for an overview of toxic or hazardous substances or elements that might be contained in product parts in concentrations above the limits defined by SJ/T 11363-2006. |

**Table 29:** Toxic or hazardous substances or elements with defined concentration limits

| 部件名称<br>Name of the part | 有毒有害物质或元素 Hazardous substances | | | | | |
|---|---|---|---|---|---|---|
| | 铅<br>(Pb) | 汞<br>(Hg) | 镉<br>(Cd) | 六价铬<br>(Cr(VI)) | 多溴联苯<br>(PBB) | 多溴二苯醚<br>(PBDE) |
| 金属部件<br>(Metal Parts) | O | O | O | O | O | O |
| 电路模块<br>(Circuit Modules) | X | O | O | O | O | O |
| 电缆及电缆组件<br>(Cables and Cable Assemblies) | O | O | O | O | O | O |
| 塑料和聚合物部件<br>(Plastic and Polymeric parts) | O | O | O | O | O | O |

O:
表示该有毒有害物质在该部件所有均质材料中的含量均在SJ/T11363-2006 标准规定的限量要求以下。
Indicates that this toxic or hazardous substance contained in all of the homogeneous materials for this part is below the limit requirement in SJ/T11363-2006.

X:
表示该有毒有害物质至少在该部件的某一均质材料中的含量超出SJ/T11363-2006标准规定的限量要求。
Indicates that this toxic or hazardous substance contained in at least one of the homogeneous materials used for this part *might exceed* the limit requirement in SJ/T11363-2006.

## 5.2 SAR requirements specific to portable mobiles

Mobile phones, PDAs or other portable transmitters and receivers incorporating a GSM module must be in accordance with the guidelines for human exposure to radio frequency energy. This requires the Specific Absorption Rate (SAR) of portable ELS61-E R2 based applications to be evaluated and approved for compliance with national and/or international regulations.

Since the SAR value varies significantly with the individual product design manufacturers are advised to submit their product for approval if designed for portable use. For European-markets the relevant directives are mentioned below. It is the responsibility of the manufacturer of the final product to verify whether or not further standards, recommendations or directives are in force outside these areas.

*Products intended for sale on European markets*

| | |
|---|---|
| EN 50360 | Product standard to demonstrate the compliance of mobile phones with the basic restrictions related to human exposure to electromagnetic fields (300MHz - 3GHz) |
| EN 62311:2008 | Assessment of electronic and electrical equipment related to human expo-sure restrictions for electromagnetic fields (0 Hz - 300 GHz) |

Please note that SAR requirements are specific only for portable devices and not for mobile devices as defined below:

- Portable device:
  A portable device is defined as a transmitting device designed to be used so that the radiating structure(s) of the device is/are within 20 centimeters of the body of the user.
- Mobile device:
  A mobile device is defined as a transmitting device designed to be used in other than fixed locations and to generally be used in such a way that a separation distance of at least 20 centimeters is normally maintained between the transmitter's radiating structure(s) and the body of the user or nearby persons. In this context, the term "fixed location" means that the device is physically secured at one location and is not able to be easily moved to another location.

## 5.3 Reference Equipment for Type Approval

The Thales reference setup submitted to type approve ELS61-E R2 (including a special approval adapter for the DSB75) is shown in the following figure[1]:

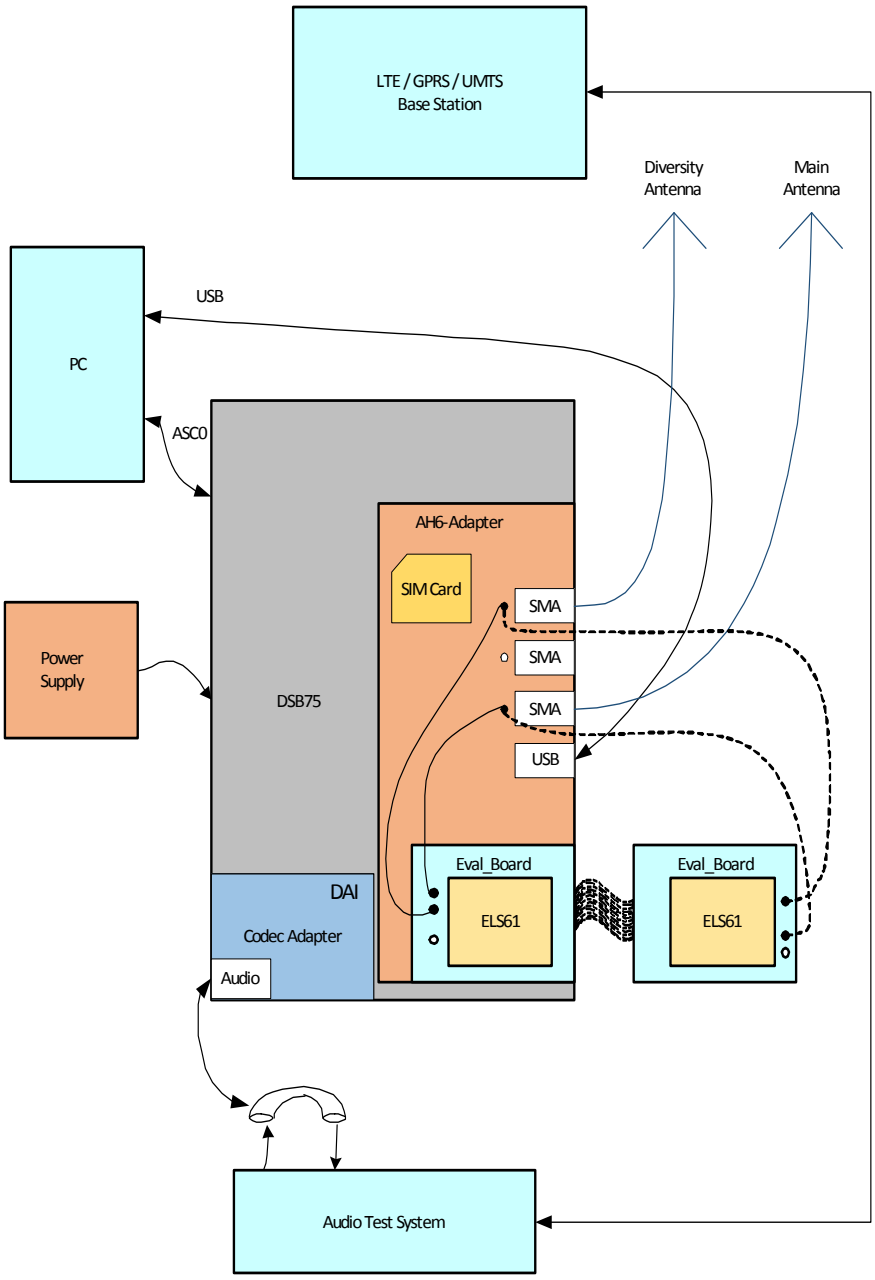



**Figure 66:** Reference equipment for Type Approval

1. For RF performance tests a mini-SMT/U.FL to SMA adapter with attached 6dB coaxial attenuator is chosen to connect the evaluation module directly to the GSM test equipment instead of employing the SMA antenna connectors on the ELS61-E R2-DSB75 adapter as shown in Figure 66. The following products are recommended:
   Hirose SMA-Jack/U.FL-Plug conversion adapter HRMJ-U.FLP(40)
   (for details see http://www.hirose-connectors.com/ or http://www.farnell.com/
   Aeroflex Weinschel Fixed Coaxial Attenuator Model 3T/4T
   (for details see http://www.aeroflex.com/ams/weinschel/pdfiles/wmod3&4T.pdf)

# 6 Document Information

## 6.1 Revision History

Preceding document: "Cinterion® ELS61-E R2 Hardware Interface Description" Version 02.000a
New document: "Cinterion® ELS61-E R2 Hardware Interface Description" Version **02.000b**

| Chapter | What is new |
|---|---|
| -- | Layout update. |

Preceding document: "Cinterion® ELS61-E R2 Hardware Interface Description" Version 02.000
New document: "Cinterion® ELS61-E R2 Hardware Interface Description" Version 02.000a

| Chapter | What is new |
|---|---|
| 3.5.1 | Added general note for current consumption rating listed in Table 18. |

Preceding document: "Cinterion® ELS61-E R2 Hardware Interface Description" Version 01.070c
New document: "Cinterion® ELS61-E R2 Hardware Interface Description" Version 02.000

| Chapter | What is new |
|---|---|
| Throughout document | Added MCLK signal (optionally configurable for GPIO4 or GPIO13). |
| 3.5.1 | Revised some power supply ratings. |
| 5.1 | Revised Table 26 regarding version of the standards |

Preceding document: "Cinterion® ELS61-E R2 Hardware Interface Description" Version 01.070b
New document: "Cinterion® ELS61-E R2 Hardware Interface Description" Version 01.070c

| Chapter | What is new |
|---|---|
| 2 | Revised figures showing startup behavior for ASC0, ASC1, GPIO, DAI, and $I^2C$. |
| 3.2.3 | Revised Table 15. |
| 3.5.1 | Revised some power supply ratings. |

Preceding document: "Cinterion® ELS61-E R2 Hardware Interface Description" Version 01.070a
New document: "Cinterion® ELS61-E R2 Hardware Interface Description" Version 01.070b

| Chapter | What is new |
|---|---|
| 2.2.1 | Revised note on Rx diversity antenna connection. |

Preceding document: "Cinterion® ELS61-E R2 Hardware Interface Description" Version 01.070
New document: "Cinterion® ELS61-E R2 Hardware Interface Description" Version 01.070a

| Chapter | What is new |
|---|---|
| 2.1.7.3 | Three sample solutions for using DAI added. |
| 5.3 | Figure 66: Reference equipment for type approval updated. |

Preceding document: "Cinterion® ELS61-E R2 Hardware Interface Description" Version 01.040a
New document: "Cinterion® ELS61-E R2 Hardware Interface Description" Version 01.070

| Chapter | What is new |
|---|---|
| 7.1 | Updated Table 30 ordering number. |
| 3.2.1.3 | New Figure 40: Automatic ON circuit added. |
| 5.1 | Revised Table 26:Standards of European type approvals. |

Preceding document: "Cinterion® ELS61-E Hardware Interface Description" Version 01.040
New document: "Cinterion® ELS61-E R2 Hardware Interface Description" Version 01.040a

| Chapter | What is new |
|---|---|
| Throughout document | Changed product name from ELS61-E to ELS61-ER2. |
| 3.2.1.3 | Updated chapter's description. |
| 3.2.1.2 | Updated Figure 39 regarding EMERG_RST. |
| 3.2.2.2 | Updated Figure 43 regarding EMERG_RST. |

Preceding document: "Cinterion® ELS61-E Hardware Interface Description" Version 01.000c
New document: "Cinterion® ELS61-E Hardware Interface Description" Version 01.040

| Chapter | What is new |
|---|---|
| Throughout document | Added DAI (PCM/$I^2S$) interface.<br>Added support for UMTS BdI and BdVIII. |
| 2.1.2 | Revised value for required ESR capacitor at $BATT+_{BB}$.<br>Revised Clmax value for V180 line.<br>Revised $V_{OL}$min for $I^2C$ (and added note). |
| 3.2.1.2 | Revised remark on application of rising edge for ON signal (timing). |

Preceding document: "Cinterion® ELS61-E Hardware Interface Description" Version 01.000b
New document: "Cinterion® ELS61-E Hardware Interface Description" Version 01.000c

| Chapter | What is new |
|---|---|
| 2.1.2 | Revised Table 2 regarding CCVCC |
| 2.1.14.4 | Added fast shutdown time in Figure 27 |
| 3.1 | Alarm mode added to Table 14 |
| 3.2.1.3 | New chapter for Power On circuits added |
| 3.2.3 | Revised Table 15 regarding signal CCIN |
| 3.5.1 | Revised measurement condition to @max power in Table 18 |
| 3.8 | Revised Table 21 for signals CCRST, CCIO, CCCLK and added VUSB, USB_DP, -DN |
| 4.2.3.1 | Revised Table 23 regarding the latest solder profile |
| 4.2.3.2 | Revised regarding changes in Table 23 |
| 5.1 | Revised Table 25 to standards used in certification |

Preceding document: "Cinterion® ELS61-E Hardware Interface Description" Version 01.000a
New document: "Cinterion® ELS61-E Hardware Interface Description" Version 01.000b

| Chapter | What is new |
|---|---|
| 2.1.2 | Update ON signal by adding the table footnote 2 in Table 2. |
| 3.2.1.2 | The input allowed for ON signal is updated as an input voltage level up to 5V.<br>The R2 value with Option 2 is updated as 3K.<br>Remove Figure 31 and Figure 32.<br>Update description of ON signal to indicate the fact that it is required to wait at least 1 second after the operating voltage is applied.<br>Update Figure 33 with 1 second delay of the rising edge of ON signal. |

Preceding document: "Cinterion® ELS61-E Hardware Interface Description" Version 01.000
New document: "Cinterion® ELS61-E Hardware Interface Description" Version 01.000a

| Chapter | What is new |
|---|---|
| 5.1 | Replaced 1999/5/EC with 2014/53/EU in Table 25.<br>Added 2014/53/EU related requirements in Table 27. |
| 5.2 | Added one more SAR requirement for Products intended for sale on European markets. |

Preceding document: "Cinterion® ELS61-E Hardware Interface Description" Version 00.301
New document: "Cinterion® ELS61-E Hardware Interface Description" Version 01.000

| Chapter | What is new |
|---|---|
| 1.1 | Description added to indicate that the HTTP/SecureConnection over SSL version 3.0 and TLS versions 1.0, 1.1, and 1.2 are supported. |
| 2.1.1 | Add description for GPIO20-23 in Figure 4 to list the reserved PCM functions for future use. |
| 2.1.2 | 1. Update $V_I$norm value in Table 2 for both power supply and external power supply as 3.8V.<br>2. Update Ignition signal in Table 2 to change the Slew rate <=1µs. Add the internal pull down value for this signal as 100kΩ.<br>3. Update CCVCC signal specification in Table 2.<br>4. Update comment of I2C signal line in Table 2. |
| 2.1.9 | Update Figure 13 to modify the startup behavior for GPIO2. |
| 2.1.10 | Add the internal pull up resistor value 1KOhm to Figure 22. |
| 2.2.1 | Update antenna interface data in Table 13. |
| 2.3 | Update Figure 27 to:<br>1. add the recommended BEAD type.<br>2. add note for I2CCLK and I2CDAT line to indicate the internal pull up resistor to V180. |
| 3.2.1.2 | The input allowed for ON signal is updated as an input voltage level up to 5V.<br>The R2 value with Option 2 is updated as 3K.<br>Add Figure 37 |
| 3.2.3 | Update signal states of I2CCLK and I2CDAT in Table 15. |
| 3.4.1 | Update current consumption ratings and its test condition in Table 17. |

Preceding document: "Cinterion® ELS61-E Hardware Interface Description" Version 00.281
New document: "Cinterion® ELS61-E Hardware Interface Description" Version 00.301

| Chapter | What is new |
|---|---|
| 3.2.4.1 | Add description for how to monitor module status by PWR_IND signal. |
| 3.4.1 | Update data in Table 17. |

New document: "Cinterion® ELS61-E Hardware Interface Description" Version 00.281

| Chapter | What is new |
|---|---|
| -- | Initial document setup. |

## 6.2 Related Documents

[1] ELS61-E R2 AT Command Set
[2] ELS61-E R2 Release Note
[3] Application Note 26: Power Supply for Wireless Applications
[4] Application Note 48: SMT Module Integration
[5] Application Note 40: Thermal Solutions
[6] Universal Serial Bus Specification Revision 2.0, April 27, 2000

## 6.3 Terms and Abbreviations

| Abbreviation | Description |
|---|---|
| ADC | Analog-to-digital converter |
| AGC | Automatic Gain Control |
| ANSI | American National Standards Institute |
| ARFCN | Absolute Radio Frequency Channel Number |
| ARP | Antenna Reference Point |
| ASC0/ASC1 | Asynchronous Controller. Abbreviations used for first and second serial interface of ELS61-E R2 |
| B | Thermistor Constant |
| BER | Bit Error Rate |
| BIP | Bearer Independent Protocol |
| BTS | Base Transceiver Station |
| CB or CBM | Cell Broadcast Message |
| CE | Conformité Européene (European Conformity) |
| CHAP | Challenge Handshake Authentication Protocol |
| CPU | Central Processing Unit |
| CS | Coding Scheme |
| CSD | Circuit Switched Data |
| CTS | Clear to Send |
| DAC | Digital-to-Analog Converter |
| dBm0 | Digital level, 3.14dBm0 corresponds to full scale, see ITU G.711, A-law |
| DCE | Data Communication Equipment (typically modems, e.g. Thales module) |
| DCS 1800 | Digital Cellular System, also referred to as PCN |
| DRX | Discontinuous Reception |
| DSB | Development Support Box |
| DSP | Digital Signal Processor |
| DSR | Data Set Ready |
| DTR | Data Terminal Ready |
| DTX | Discontinuous Transmission |
| EFR | Enhanced Full Rate |
| EGSM | Enhanced GSM |
| EIRP | Equivalent Isotropic Radiated Power |
| EMC | Electromagnetic Compatibility |
| ERP | Effective Radiated Power |
| ESD | Electrostatic Discharge |
| ETS | European Telecommunication Standard |

| Abbreviation | Description |
|---|---|
| ETSI | European Telecommunication Standards Institute |
| FCC | Federal Communications Commission (U.S.) |
| FDMA | Frequency Division Multiple Access |
| FR | Full Rate |
| GMSK | Gaussian Minimum Shift Keying |
| GPIO | General Purpose Input/Output |
| GPRS | General Packet Radio Service |
| GSM | Global Standard for Mobile Communications |
| HiZ | High Impedance |
| HR | Half Rate |
| I/O | Input/Output |
| IC | Integrated Circuit |
| IMEI | International Mobile Equipment Identity |
| ISO | International Standards Organization |
| ITU | International Telecommunications Union |
| kbps | kbits per second |
| LED | Light Emitting Diode |
| Li-Ion/Li+ | Lithium-Ion |
| Li battery | Rechargeable Lithium Ion or Lithium Polymer battery |
| LPM | Link Power Management |
| Mbps | Mbits per second |
| MMI | Man Machine Interface |
| MO | Mobile Originated |
| MS | Mobile Station (GSM module), also referred to as TE |
| MSISDN | Mobile Station International ISDN number |
| MT | Mobile Terminated |
| NTC | Negative Temperature Coefficient |
| OEM | Original Equipment Manufacturer |
| PA | Power Amplifier |
| PAP | Password Authentication Protocol |
| PBCCH | Packet Switched Broadcast Control Channel |
| PCB | Printed Circuit Board |
| PCL | Power Control Level |
| PCM | Pulse Code Modulation |
| PCN | Personal Communications Network, also referred to as DCS 1800 |
| PCS | Personal Communication System, also referred to as GSM 1900 |
| PDU | Protocol Data Unit |

| Abbreviation | Description |
|---|---|
| PLL | Phase Locked Loop |
| PPP | Point-to-point protocol |
| PSK | Phase Shift Keying |
| PSU | Power Supply Unit |
| PWM | Pulse Width Modulation |
| R&TTE | Radio and Telecommunication Terminal Equipment |
| RAM | Random Access Memory |
| RF | Radio Frequency |
| RLS | Radio Link Stability |
| RMS | Root Mean Square (value) |
| RoHS | Restriction of the use of certain hazardous substances in electrical and electronic equipment. |
| ROM | Read-only Memory |
| RTC | Real Time Clock |
| RTS | Request to Send |
| Rx | Receive Direction |
| SAR | Specific Absorption Rate |
| SAW | Surface Accoustic Wave |
| SELV | Safety Extra Low Voltage |
| SIM | Subscriber Identification Module |
| SMD | Surface Mount Device |
| SMS | Short Message Service |
| SMT | Surface Mount Technology |
| SPI | Serial Peripheral Interface |
| SRAM | Static Random Access Memory |
| TA | Terminal adapter (e.g. GSM module) |
| TDMA | Time Division Multiple Access |
| TE | Terminal Equipment, also referred to as DTE |
| TLS | Transport Layer Security |
| Tx | Transmit Direction |
| UART | Universal asynchronous receiver-transmitter |
| URC | Unsolicited Result Code |
| USSD | Unstructured Supplementary Service Data |
| VSWR | Voltage Standing Wave Ratio |

## 6.4 Safety Precaution Notes

The following safety precautions must be observed during all phases of the operation, usage, service or repair of any cellular terminal or mobile incorporating ELS61-E R2. Manufacturers of the cellular terminal are advised to convey the following safety information to users and operating personnel and to incorporate these guidelines into all manuals supplied with the product. Failure to comply with these precautions violates safety standards of design, manufacture and intended use of the product. Thales assumes no liability for customer's failure to comply with these precautions.

| | |
|---|---|
|  | When in a hospital or other health care facility, observe the restrictions on the use of mobiles. Switch the cellular terminal or mobile off, if instructed to do so by the guidelines posted in sensitive areas. Medical equipment may be sensitive to RF energy. The operation of cardiac pacemakers, other implanted medical equipment and hearing aids can be affected by interference from cellular terminals or mobiles placed close to the device. If in doubt about potential danger, contact the physician or the manufacturer of the device to verify that the equipment is properly shielded. Pacemaker patients are advised to keep their hand-held mobile away from the pacemaker, while it is on. |
|  | Switch off the cellular terminal or mobile before boarding an aircraft. Make sure it cannot be switched on inadvertently. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communications systems. Failure to observe these instructions may lead to the suspension or denial of cellular services to the offender, legal action, or both. |
|  | Do not operate the cellular terminal or mobile in the presence of flammable gases or fumes. Switch off the cellular terminal when you are near petrol stations, fuel depots, chemical plants or where blasting operations are in progress. Operation of any electrical equipment in potentially explosive atmospheres can constitute a safety hazard. |
|  | Your cellular terminal or mobile receives and transmits radio frequency energy while switched on. Remember that interference can occur if it is used close to TV sets, radios, computers or inadequately shielded equipment. Follow any special regulations and always switch off the cellular terminal or mobile wherever forbidden, or when you suspect that it may cause interference or danger. |
|  | Road safety comes first! Do not use a hand-held cellular terminal or mobile when driving a vehicle, unless it is securely mounted in a holder for speakerphone operation. Before making a call with a hand-held terminal or mobile, park the vehicle. Speakerphones must be installed by qualified personnel. Faulty installation or operation can constitute a safety hazard. |
|  | IMPORTANT!<br>Cellular terminals or mobiles operate using radio signals and cellular networks. Because of this, connection cannot be guaranteed at all times under all conditions. Therefore, you should never rely solely upon any wireless device for essential communications, for example emergency calls.<br>Remember, in order to make or receive calls, the cellular terminal or mobile must be switched on and in a service area with adequate cellular signal strength.<br>Some networks do not allow for emergency calls if certain network services or phone features are in use (e.g. lock functions, fixed dialing etc.). You may need to deactivate those features before you can make an emergency call.<br>Some networks require that a valid SIM card be properly inserted in the cellular terminal or mobile. |

# 7 Appendix

## 7.1 List of Parts and Accessories

**Table 30:** List of parts and accessories

| Description | Supplier | Ordering information |
|---|---|---|
| ELS61-E R2 | Thales | Standard module<br>Thales IMEI:<br>Packaging unit (ordering) number: L30960-N4450-A200<br>Module label number: S30960-S4450-A200-1[1] |
| ELS61-E R2 Evaluation Module | Thales | Ordering number: L30960-N4451-A200(ELS61-ER2) |
| DSB75 Evaluation Kit | Thales | Ordering number: L36880-N8811-A100 |
| DSB Mini Compact Evaluation Board | Thales | Ordering number: L30960-N0030-A100 |
| Starter Kit B80 | Thales | Ordering Number L30960-N0040-A100 |
| Approval adapter for mounting ELS61-E R2 evaluation modules onto DSB75 | Thales | Ordering number: L30960-N2301-A100 |
| SIM card holder incl. push button ejector and slide-in tray | Molex | Ordering numbers: 91228<br>91236<br>Sales contacts are listed in Table 31. |

1. Note: At the discretion of Thales, module label information can either be laser engraved on the module's shielding or be printed on a label adhered to the module's shielding.

**Table 31:** Molex sales contacts (subject to change)

| | | |
|---|---|---|
| Molex<br>For further information please click:<br>http://www.molex.com | Molex Deutschland GmbH<br>Otto-Hahn-Str. 1b<br>69190 Walldorf<br>Germany<br>Phone: +49-6227-3091-0<br>Fax: +49-6227-3091-8100<br>Email: mxgermany@molex.com | American Headquarters<br>Lisle, Illinois 60532<br>U.S.A.<br>Phone: +1-800-78MOLEX<br>Fax: +1-630-969-1352 |
| Molex China Distributors<br>Beijing,<br>Room 1311, Tower B, COFCO Plaza<br>No. 8, Jian Guo Men Nei Street, 100005<br>Beijing<br>P.R. China<br>Phone: +86-10-6526-9628<br>Fax: +86-10-6526-9730 | Molex Singapore Pte. Ltd.<br>110, International Road<br>Jurong Town,<br>Singapore 629174<br><br>Phone: +65-6-268-6868<br>Fax: +65-6-265-6044 | Molex Japan Co. Ltd.<br>1-5-4 Fukami-Higashi,<br>Yamato-City,<br>Kanagawa, 242-8585<br>Japan<br><br>Phone: +81-46-265-2325<br>Fax: +81-46-265-2365 |

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