# FBs-7SG2

Introduction

FBs-7SG2 is one of the LED display control modules of FBs-PLC series. One 7SG2 module can support up to 16 digits of seven-segment LED display (include decimal point) or 8 digits of 16-segment alphanumerical LED display or 128 independent LED displays. The driving voltage of this module is selectable from 2.4V~11.7V in order to meet the requirement of driving different size of LED display. The display pattern can be controlled directly by setting the content of output register. For the application involved the leading zero effect or 16 segment alphanumerical display, can use the TDSP function instruction for assistance.
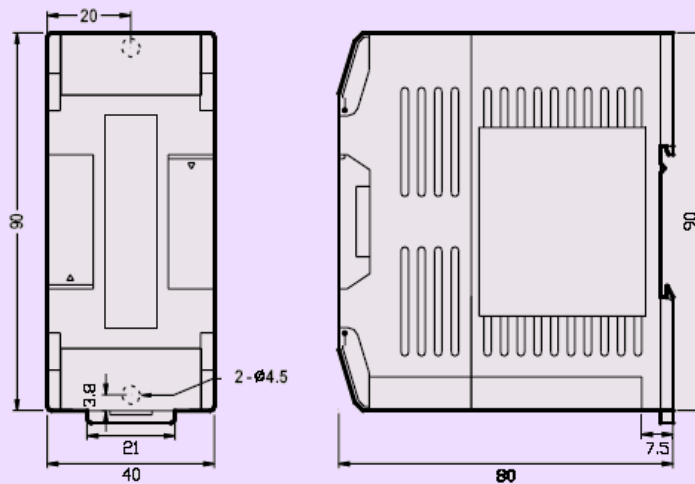
Specification

Display Mode- Decoded and Non-Decoded

Display Duty Cycle- 1/8

Update Rate- 3 mS

Control Capability-

16 digits of seven-segment LED display(include decimal point) or 8 digits of 16 segment alphanumerical LED display or 128 independent LED displays

I/O Points Occupied–

Decode- 5 output register (OR)

Non-Decode- 8 output register (OR)

Signal Connector- 16 Pin IDC connector

LED Driving Method- Common cathode

LED Driving Voltage- 2.4V~11.7V selectable

Isolation- Transformer(Power) and photo-coupler(Signal)

Indicators-

5V PWR internal power LED

EXT PWR external power LED

OV Over driving voltage LED

External Power - 24V-15%/+20%, 410mA

Internal Power Consumption - 5V, 14mA

Operating Temperature- 0 ~ 60 ℃

Storage Temperature- -20 ~ 80 ℃

Dimensions- 40(W)x90(H)x80(D) mm

## Dimension

FBs-7SG2

Signal of Connector

Display Connector

Pin	Signal Name	Pin	Signal Name
1	DIG0	2	DIG1
3	DIG2	4	DIG3
5	DIG4	6	DIG5
7	DIG6	8	DIG7
9	A/D0	10	B/D1
11	C/D2	12	D/D3
13	E/D4	14	F/D5
15	G/D6	16	P/D7

There are 2 sets of display driver in 7SG2 module. Each display driver is responsible for 64 segments of ouput and provides the connection to display module thru 16 pin IDC connector. While operation, the 64 segment outputs of LED will be multiplexed into the A/D0~P/D7 lines. The DIG0~DIG7 signals are low active output (Sink or NPN) for digit selection.

External Power Connector

This is a 3-pin euro connector and used for external 24V power connection.
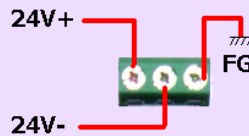
Display Control

The segment output of display is controlled by the contents of output registers. The relation between segment output and the output register depends on the working mode of display module.

Non-Decoded Mode

Under this working mode, there are 8 output registers used for the control of 128 segments. Each segment is controlled by one corresponding bit. When the bit is on, the LED is lit. The mapping of output register and segment is shown at below. In the following table, OR stands for the first output register allocated for this display control module. The 128 segments are divided into 2 channel, each channel controls 64 segments.

Output Register			
CH0	*CH1*	**D15~D8**	**D7~D0**
OR+0	**OR+4**	SEG15~SEG8	SEG7~SEG0
OR+1	**OR+5**	SEG31~SEG24	SEG23~SEG16
OR+2	**OR+6**	SEG47~SEG40	SEG39~SEG32
OR+3	**OR+7**	SEG63~SEG56	SEG63~SEG48

Segment of Display module

In order to ease the application of 7SG display module, The FBs-PLC series provides different size of seven segment (for pure digit number) and 16 segment(for alphanumerical) LED display module for user selection. The segment mapping of each type of displays are described at below.

The segment mapping of seven-segment display
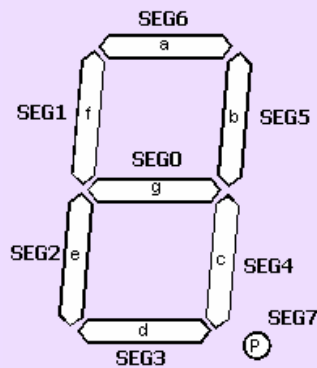
The driving signal of right most digit of display board is mapped to SEG0~SEG7 segment output and the next digit is SEG8~SEG15 while the left most one digit is SEG63~SEG56. One 7SG1 module can control 8 digits of seven-segment display.

The mapping of 16-segment display

The D0~D15 of right most digit of alphanumerical display board is mapped to SEG0~SEG15 while the D0~D15 of the left most digit is mapped to SEG63~SEG48. One 7SG2 module can control 8 digits of 16-segment display.
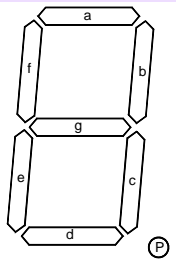
FBs-7SG2　LED Display Control Module

Decoded Mode

Under this working mode, there are 4 output registers assigned for the control of 8 digits. Each digit is controlled by four corresponding bit. Besides, there is one register assigned for the control of decimal point. Each decimal point is controlled by one corresponding bit. The mapping of output register, digit and decimal point is depicted at below, where OR represent the first output register allocated for the display module.

Class	Output Register	D15~D12	D11~D8	D7~D4	D3~D0
Common	**OR+0**	P15~P8		P7~P0	
CH0	**OR+1**	DIG3	DIG2	DIG1	DIG0
	OR+2	DIG7	DIG6	DIG5	DIG4
CH1	**OR+3**	DIG3	DIG2	DIG1	DIG0
	OR+4	DIG7	DIG6	DIG5	DIG4

The first output register controls the decimal point display. If the bit is on, the corresponding decimal point will be lit. The second to fifth output register control the 8 digits of seven-segment display. Each digit is controlled by 4 bits.

The seven-segment display pattern

Nibble value		Seven-segment structure	dark（0）lit（1）							pattern
Hex	Binary		a	b	c	d	e	f	g	
0	0000		1	1	1	1	1	1	0	0
1	0001		0	1	1	0	0	0	0	1
2	0010		1	1	0	1	1	0	1	2
3	0011		1	1	1	1	0	0	1	3
4	0100		0	1	1	0	0	1	1	4
5	0101		1	0	1	1	0	1	1	5
6	0110		1	0	1	1	1	1	1	6
7	0111		1	1	1	0	0	1	0	7
8	1000		1	1	1	1	1	1	1	8
9	1001		1	1	1	1	0	1	1	9
A	1010		0	0	0	0	0	0	1	-
B	1011		1	0	0	1	1	1	1	E
C	1100		0	1	1	0	1	1	1	H
D	1101		0	0	0	1	1	0	1	C
E	1110		0	0	0	1	1	1	1	t
F	1111		0	0	0	0	0	0	0	

FBs-7SG2　　**LED Display Control Module**

Jumper Setting
Jumper location and function

Class	Jumper	Function
Common	**JP2**	Decode(D short)/Non-decode(Open) setup
	JP3	O.V. test(T)or Normal(N) setup
	JP1	High driving voltage selection (rear panel)
C H 0	**JP5**	High(HV)/Low(LV) driving voltage selection
	JP6	0.6V(0.6V) fine voltage adjust
	JP7	1.2V(1V2) fine voltage adjust
C H 1	**JP8**	High(HV)/Low(LV) driving voltage selection
	JP9	0.6V(0.6V) fine voltage adjust
	JP10	1.2V(1V2) fine voltage adjust
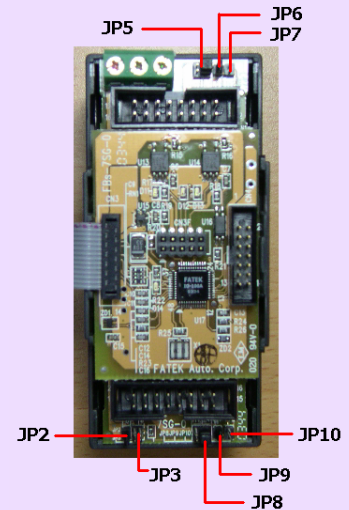
JP5/JP8	JP1	JP7/JP10	JP6/JP9	Driving voltage
LV	無關	open	open	2.4V
		open	short	3V
		short	open	3.6V
		short	short	4.2V
HV	7.5V	open	open	4.9V
		open	short	5.5V
		short	open	6.1V
		short	short	6.7V
	10V	open	open	7.4V
		open	short	8V
		short	open	8.6V
		short	short	9.2V
	12.5V	open	open	9.9V
		open	short	10.5V
		short	open	11.1V
		short	short	11.7V

The jumper cap of the JP5/JP8 should be inserted with the altitude of the handle cavity in horizon.
The JP1 juper is located at the rear side of the module.
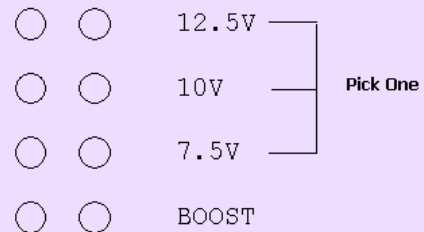
The upper three jumpers can only be jumped by one jumper cap at one time.
If the BOOST jumper is shorted, the driving voltage will be increased by 5%. This can be used for the compensation of long wire voltage drop.

Driving Voltage Selection

Due to the different driving voltage requirement for different size of LED display, selection of the proper driving voltage is the first thing that must be done. Improper driving voltage setting will let the LED brightness too dark if the voltage is too low or even blow the display module if the driving voltage is too high. When select the driving voltage of CH0, please setup the JP5~JP7 location, while CH1 please setup the JP8~JP10 location .The selection procedure is described at below:

1. Put the jumper cap of JP3 into T position to enable the over voltage test. At this moment, all LED will be lit.
2. Lookup the above selection table and start with the low voltage and gradually increase the driving voltage until the brightness is satisfied or O.V LED is turn on. If the O.V is on then should decrease the driving voltage until it goes off.
3. Put the JP3 back to the N position.